

NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P1V" represents connection to the +1.1V FPGA power plane
2. The netname "P1P1V_FIL" represents connection to the +1.1V filtered FPGA power plane
3. The netname "P1P1V_M" represents connection to the +1.1V Master ASIC power plane
4. The netname "P1P1V_S" represents connection to the +1.1V Slave ASIC power plane
5. The netname "P1P15V" represents connection to the +1.15V FPGA power plane
6. The netname "P1P15V_FIL" represents connection to the +1.15V filtered FPGA power plane
7. The netname "P1P15V_M" represents connection to the +1.15V Master ASIC power plane
8. The netname "P1P15V_S" represents connection to the +1.15V Slave ASIC power plane
9. The netname "P1P8V_M" represents connection to the +1.8V Master ASIC power plane
10. The netname "P1P8V_S" represents connection to the +1.8V Slave ASIC power plane
11. The netname "A1P8V_M" represents connection to the +1.8V Master ASIC power plane for the PLLs
12. The netname "A1P8V_S" represents connection to the +1.8V Slave ASIC power plane for the PLLs
13. The netname "P2P5V" represents connection to the +2.5V FPGA power plane
14. The netname "P2P5V_FIL" represents connection to the +2.5V filtered FPGA power plane
15. The netname "P2P5V_M" represents connection to the +2.5V Master ASIC power plane
16. The netname "P2P5V_S" represents connection to the +2.5V Slave ASIC power plane
17. The netname "P3P3V" represents connection to the +3.3V FPGA power plane
18. The netname "P3P3V_M" represents connection to the +3.3V Master ASIC power plane
19. The netname "P3P3V_S" represents connection to the +3.3V Slave ASIC power plane
20. The netname "P5V_M" represents connection to the +5V Master ASIC power plane
21. The netname "P5V_S" represents connection to the +5V Slave ASIC power plane
22. The netname "P12V" represents the connection to the +12.0V power plane.
23. The netname "GND" represents connection to the ground plane
24. A "Z" suffix on a signal name indicates an active low signal
25. All components with designators "U*", "Q*", "D*" are electrostatic discharge sensitive.
26. All components with designators above 500 are mounted on the bottom side of the board.
27. All resistor values are in ohms.

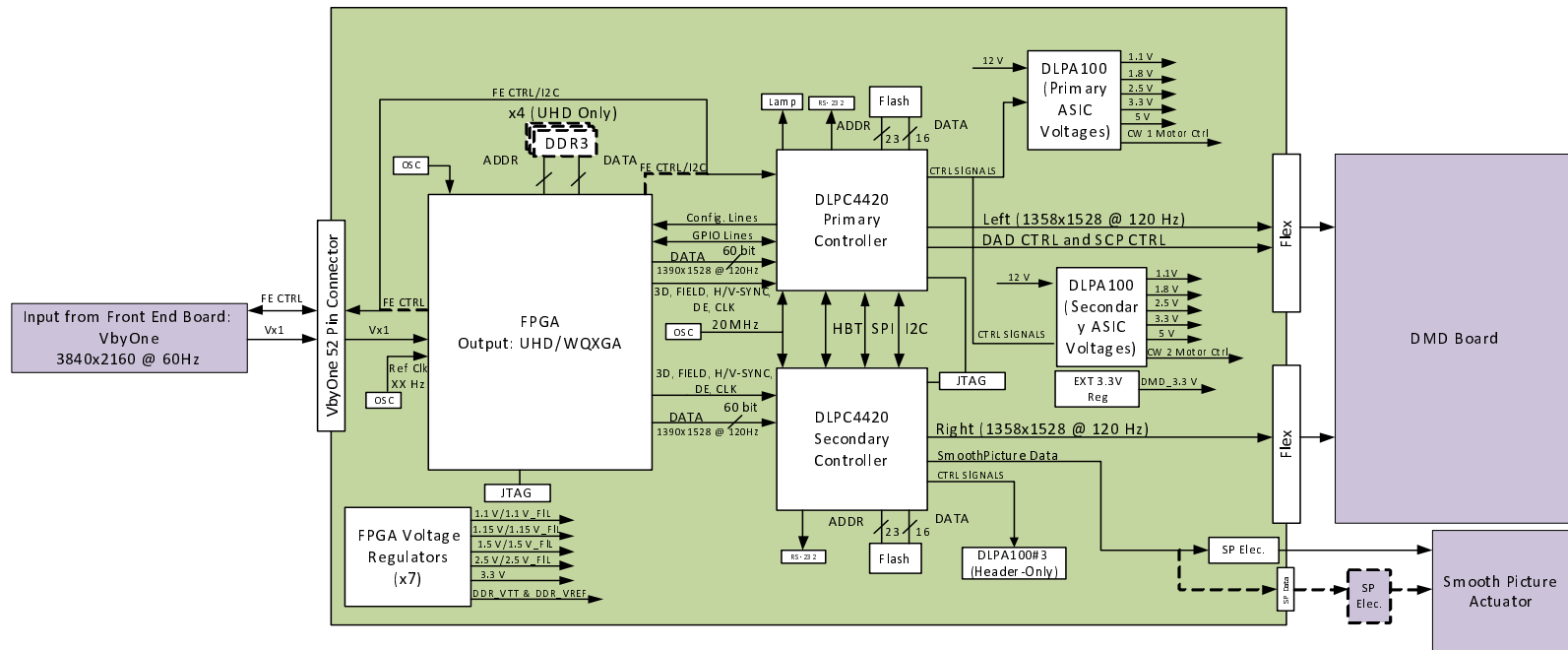


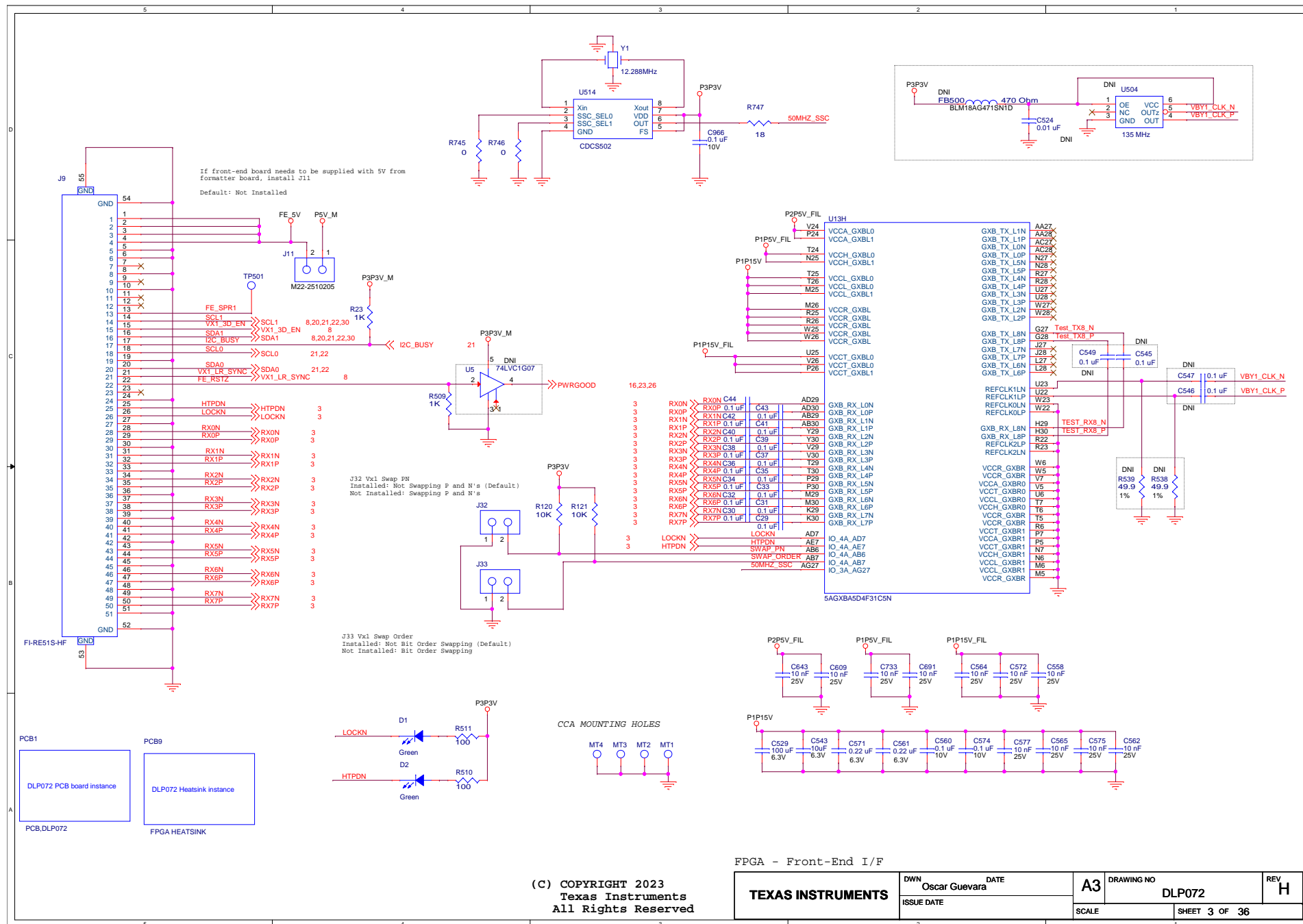
INDEX

Sheet 1: Cover
Sheet 2: Block Diagram
Sheet 3: FPGA Front End I/F
Sheet 4: FPGA DDR3 I/F
Sheet 5: DDR3 Memory 1&2
Sheet 6: DDR3 Memory 3&4
Sheet 7: FPGA Video Out I/F
Sheet 8: FPGA Programming/Test MUX
Sheet 9: FPGA Power
Sheet 10: FPGA Regulators
Sheet 11: FPGA Regulators
Sheet 12: FPGA Ground
Sheet 13: ASIC Video Input I/F
Sheet 14: Primary DMD Flex I/F
Sheet 15: Secondary DMD Flex I/F
Sheet 16: Input Power and PMD1000 I/F
Sheet 17: Primary DLPAL100 Power Supplies
Sheet 18: Secondary DLPAL100 Power Supplies
Sheet 19: ColorWheel Drive
Sheet 20: Fans, CW Index, Peripheral Connectors
Sheet 21: Primary ASIC GPIO, I2C, and Lamp Ballast
Sheet 22: GPIO Expander, Keypad Interface and IR
Sheet 23: Primary ASIC TP, ARM JTAG, RESET
Sheet 24: Secondary ASIC TP, ARM JTAG
Sheet 25: Primary RS-232, SPI, and USB
Sheet 26: Primary ASIC Flash I/F
Sheet 27: Secondary ASIC Flash I/F
Sheet 28: ASIC SSI I/F
Sheet 29: SSI Driver I/F
Sheet 30: Secondary ASIC GPIO & Smooth Picture I/F
Sheet 31: Smooth Picture Electronics
Sheet 32: Primary Power and Bypass Caps
Sheet 33: Secondary Power and Bypass Caps
Sheet 34: Output FMC Connector
Sheet 35: Revision History
Sheet 36: Important Notice

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		ENGR Oscar Guevara			
		SYST			
		PRJ			
		QA		TITLE DLPC4420A Controller Board	
NEXT ASSY	USED ON			A3	DRAWING NO DLP072
APPLICATION		SW	Cadence Capture V.16.6	SCALE	SHEET 1 of 36
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Block Diagram

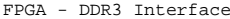




FPGA - Front-End I/F

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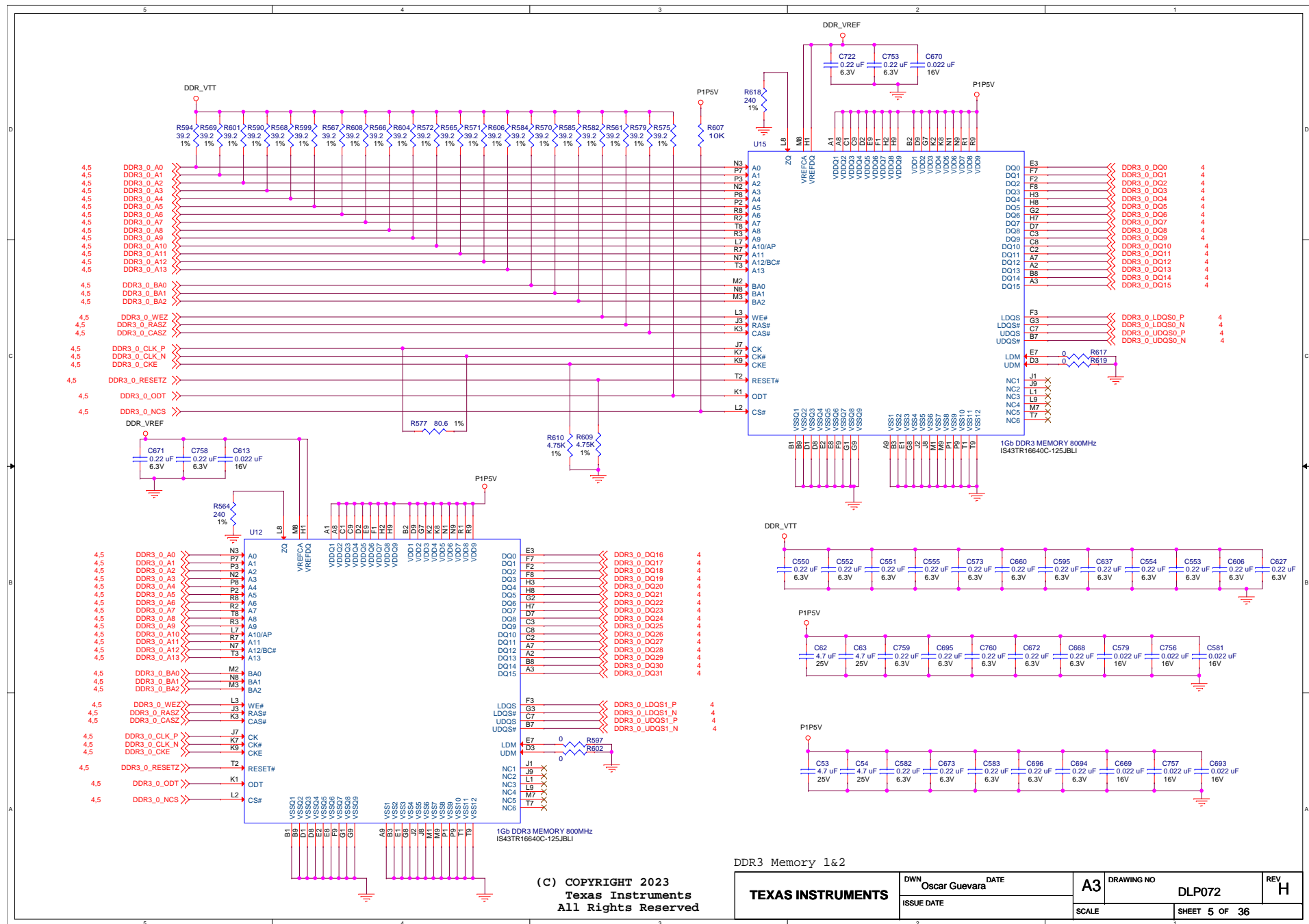
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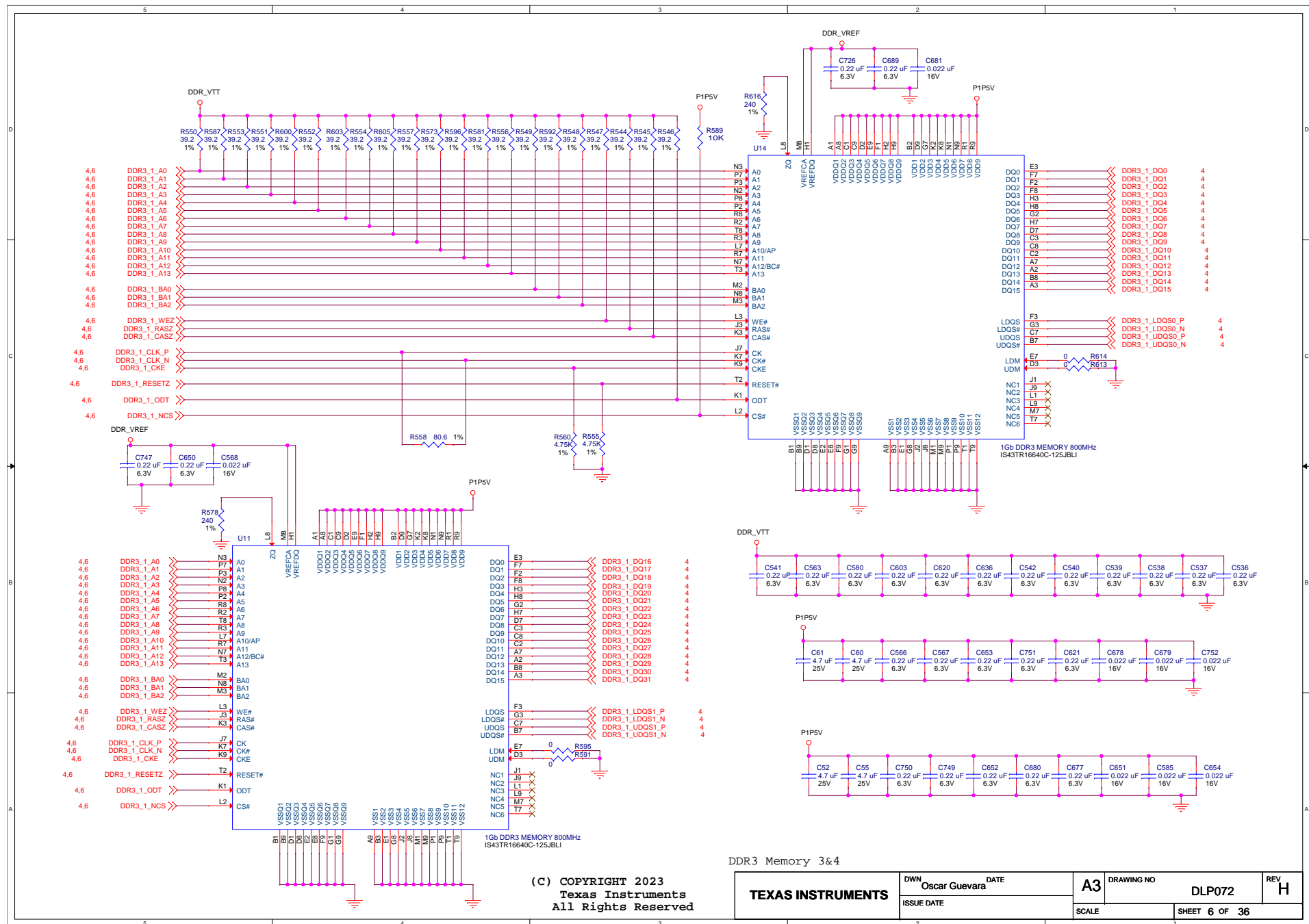
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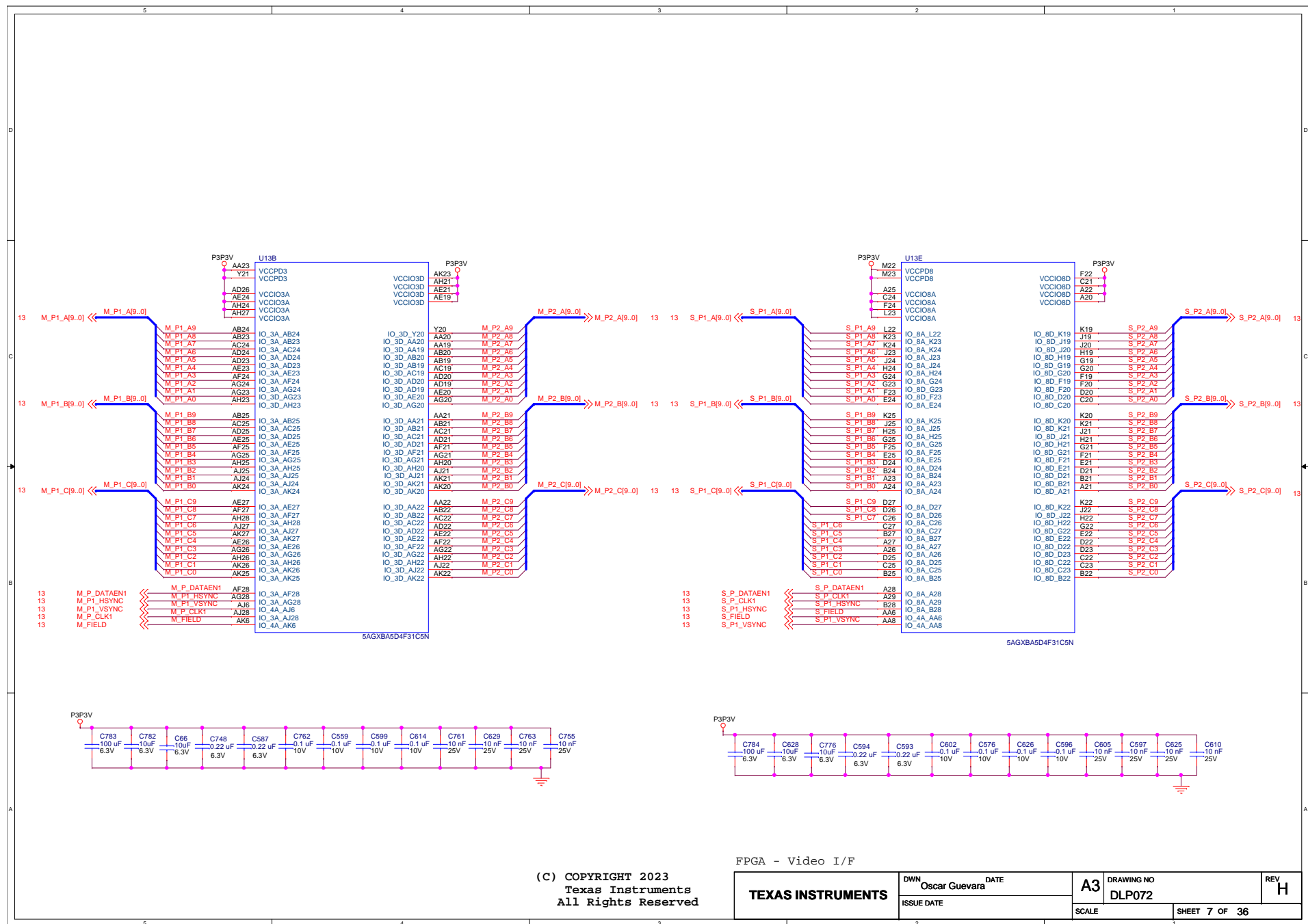
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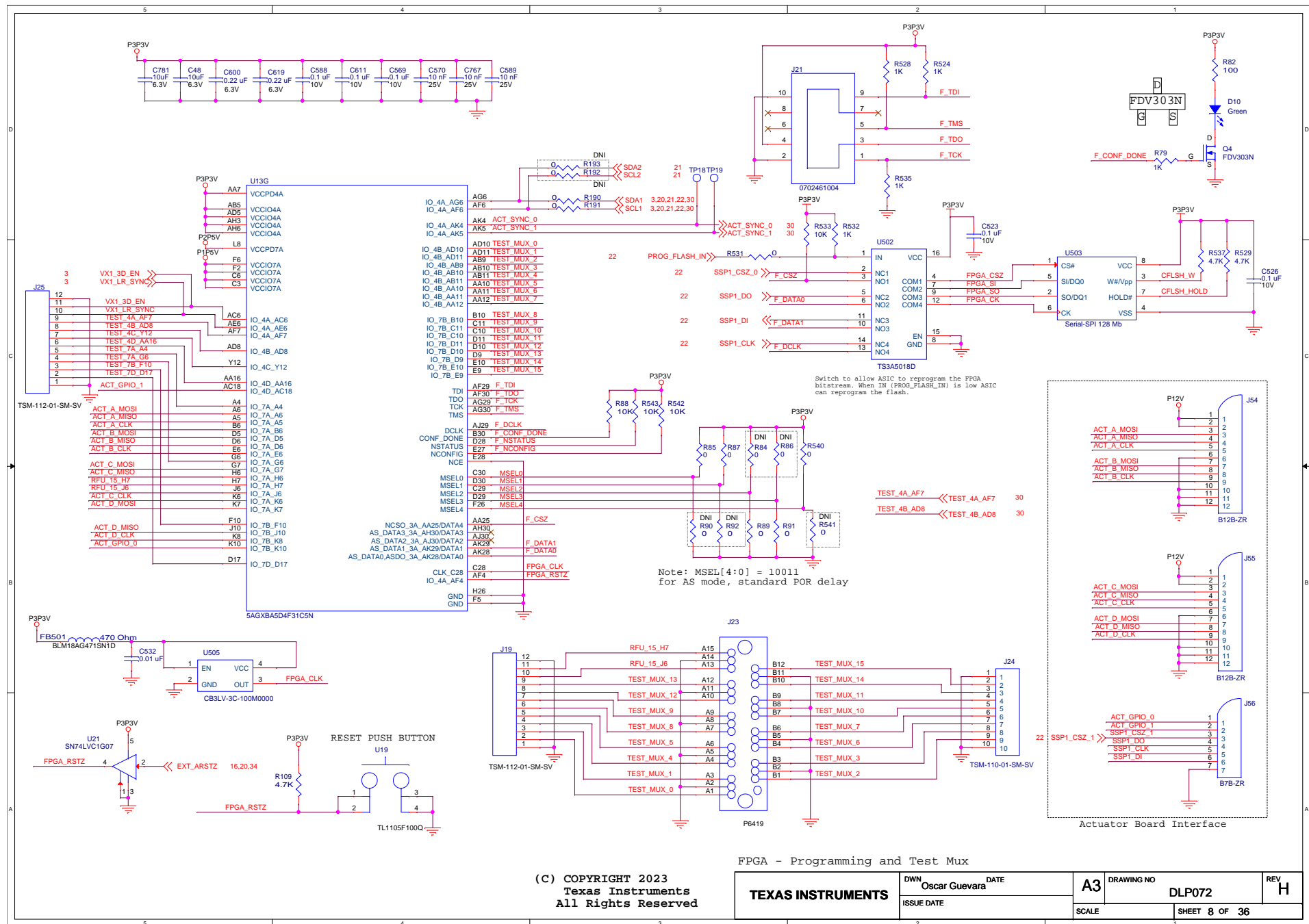


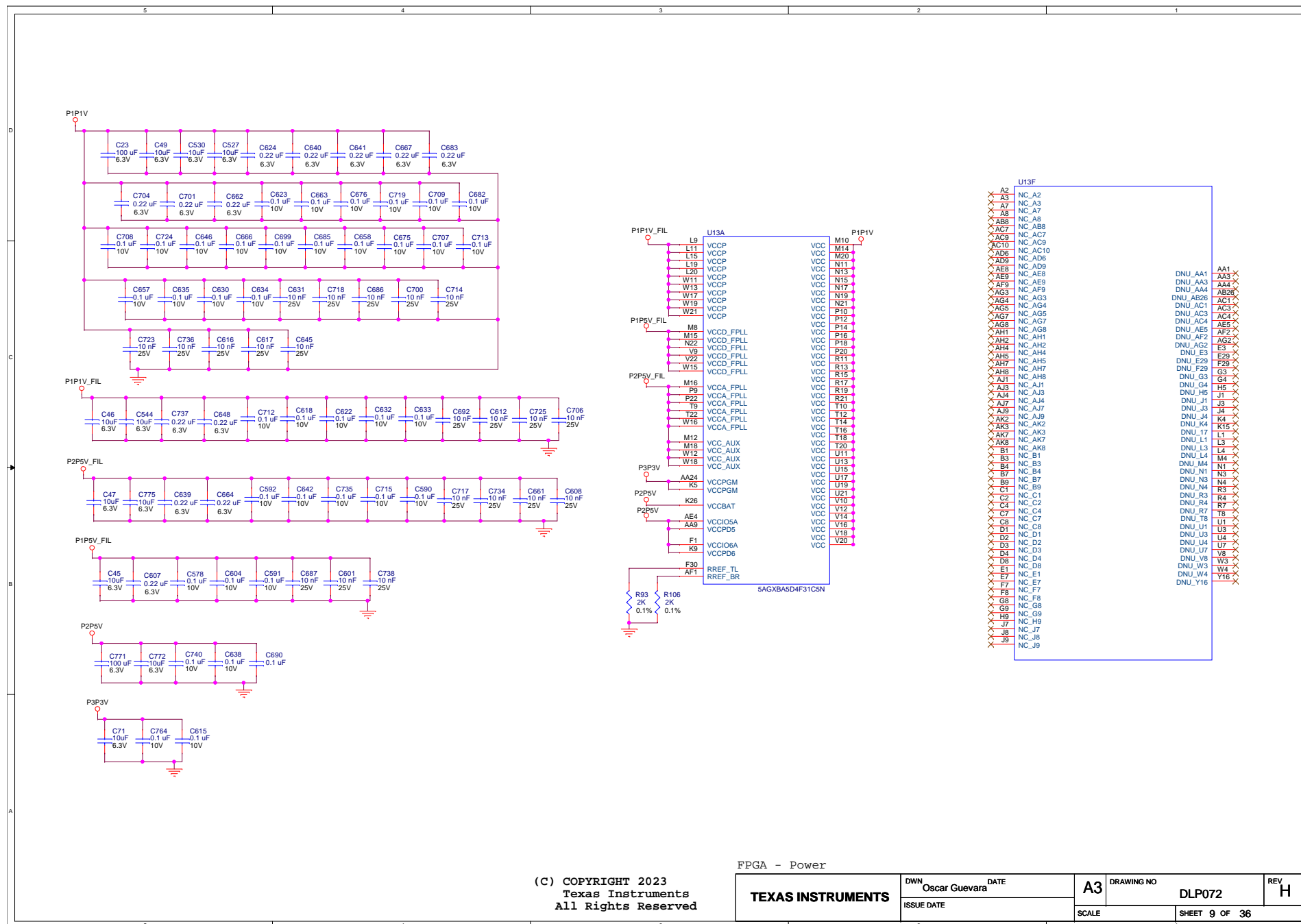
DDR3 Memory 1&2

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FPGA - Power

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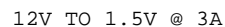
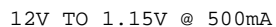
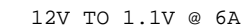
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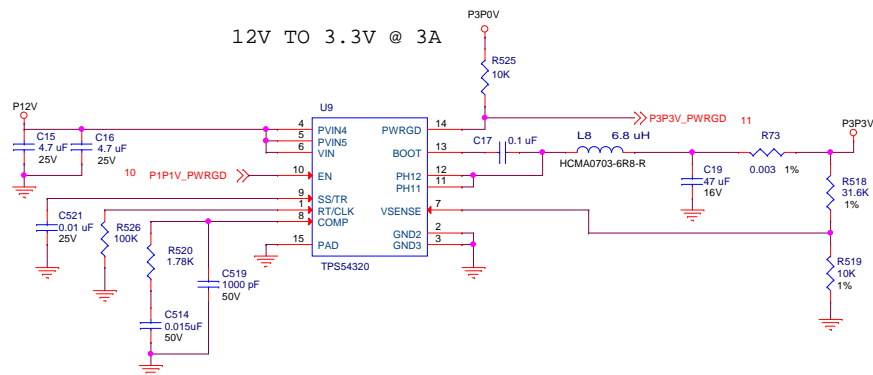
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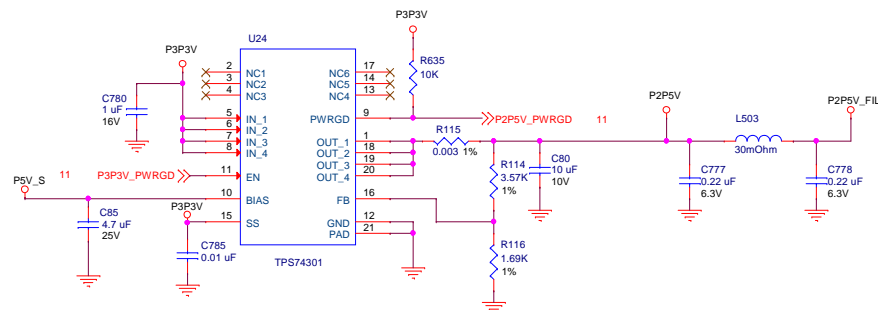
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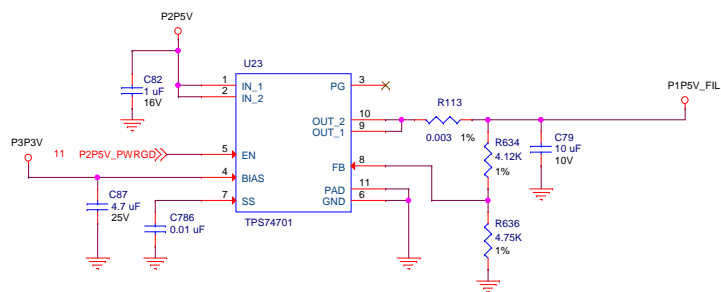
12V TO 3.3V @ 3A



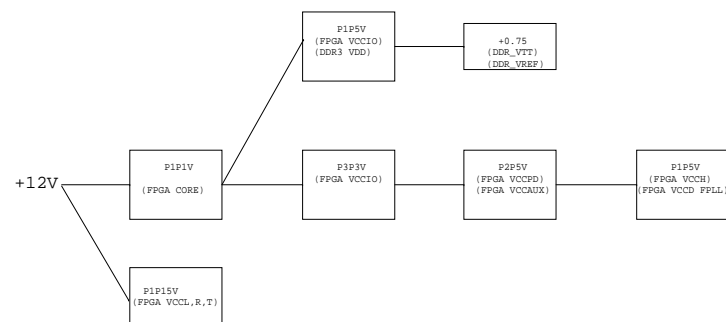
3.3V TO 2.5V @ 1.5A



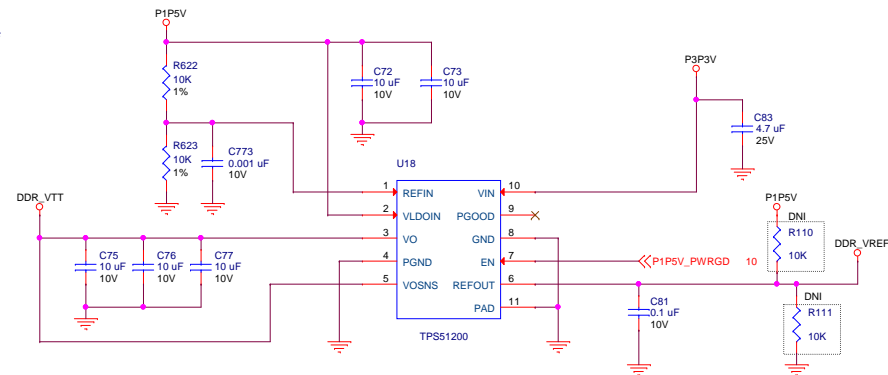
2.5V TO 1.5V @ 500mA



Power Sequence



1.5V TO 0.75V DDR_VTT & DDR_VREF



DDR TERMINATION VOLTAGE

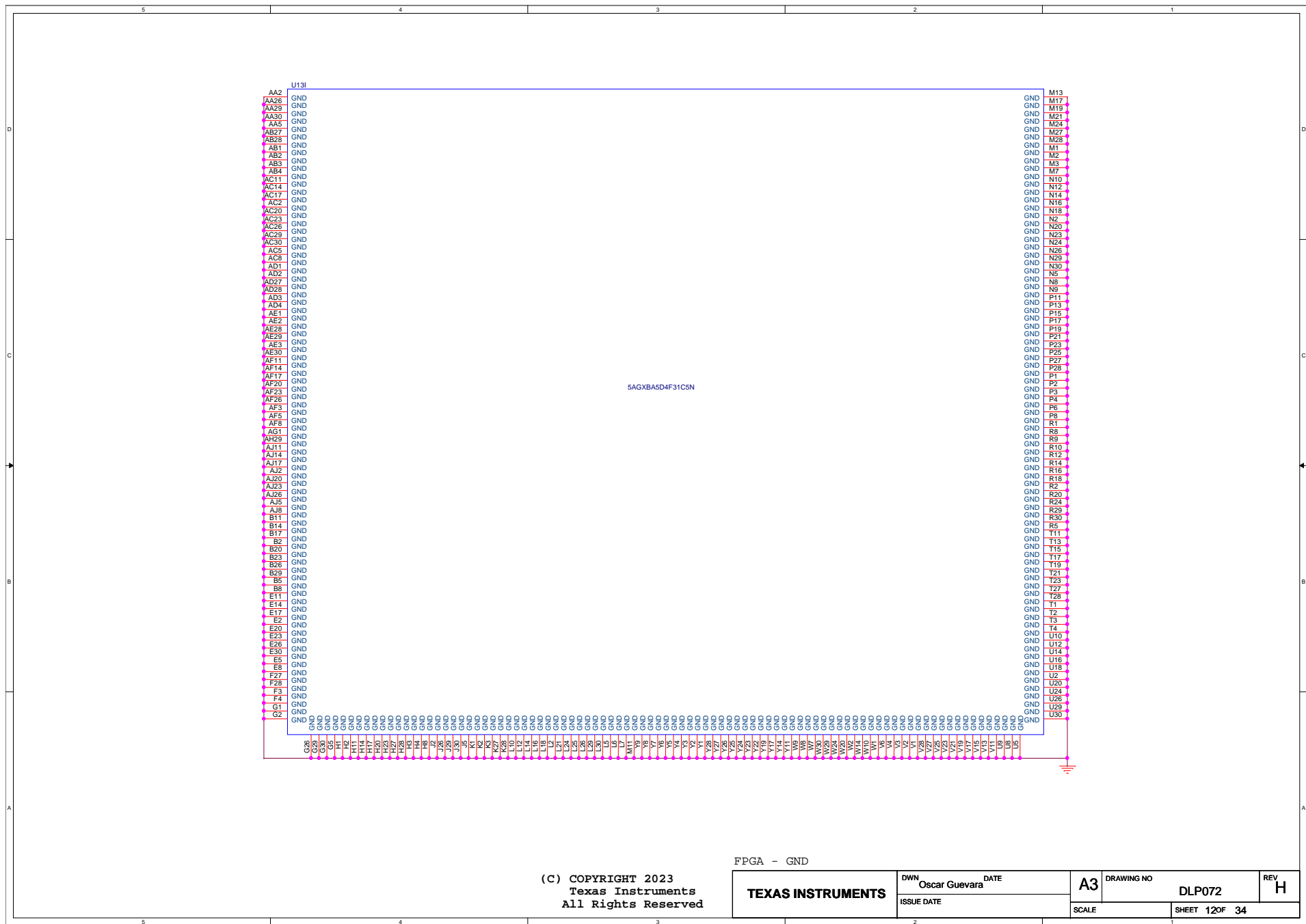
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FPGA - Regulators

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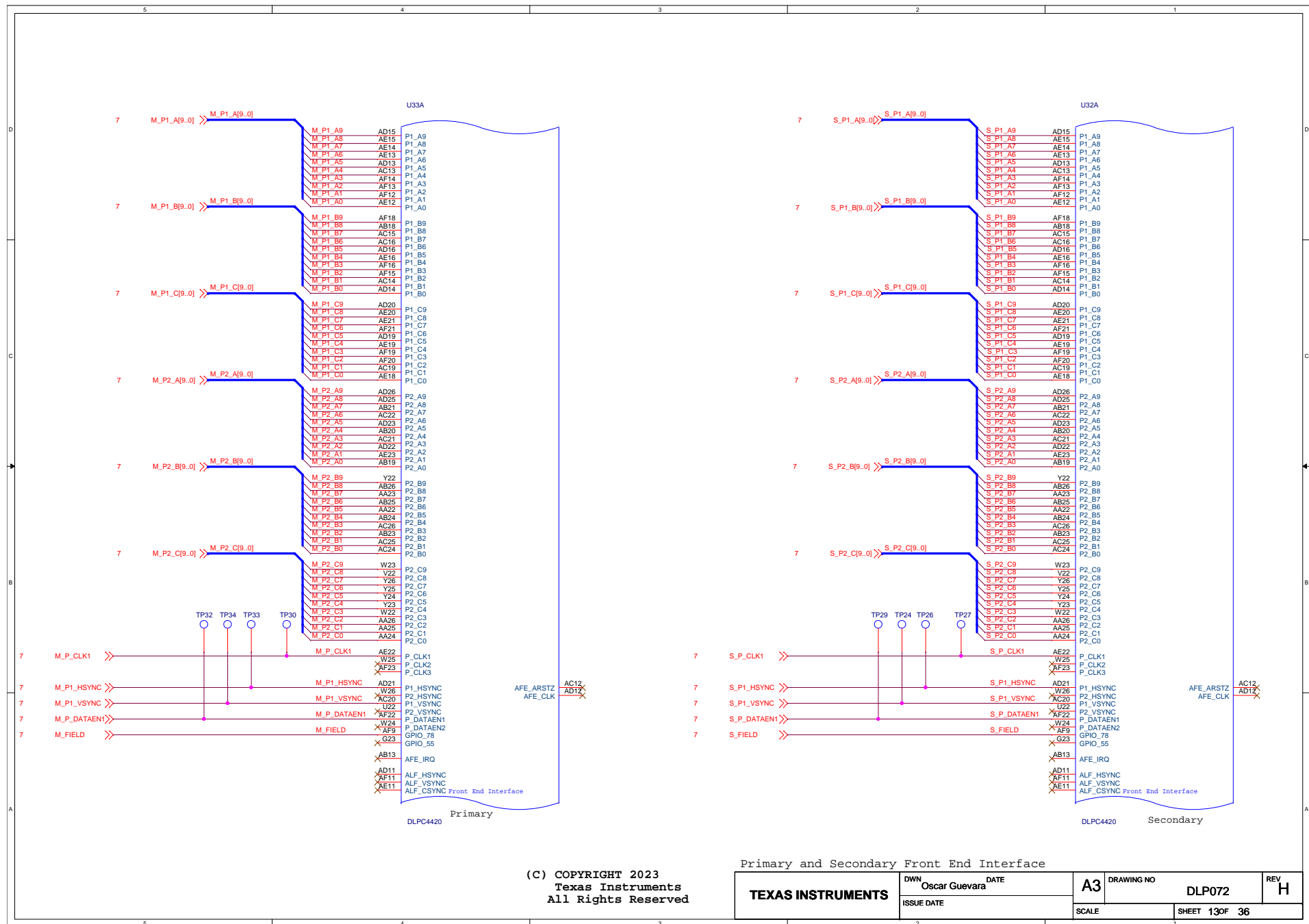
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SCALE	SHEET 110F		36	



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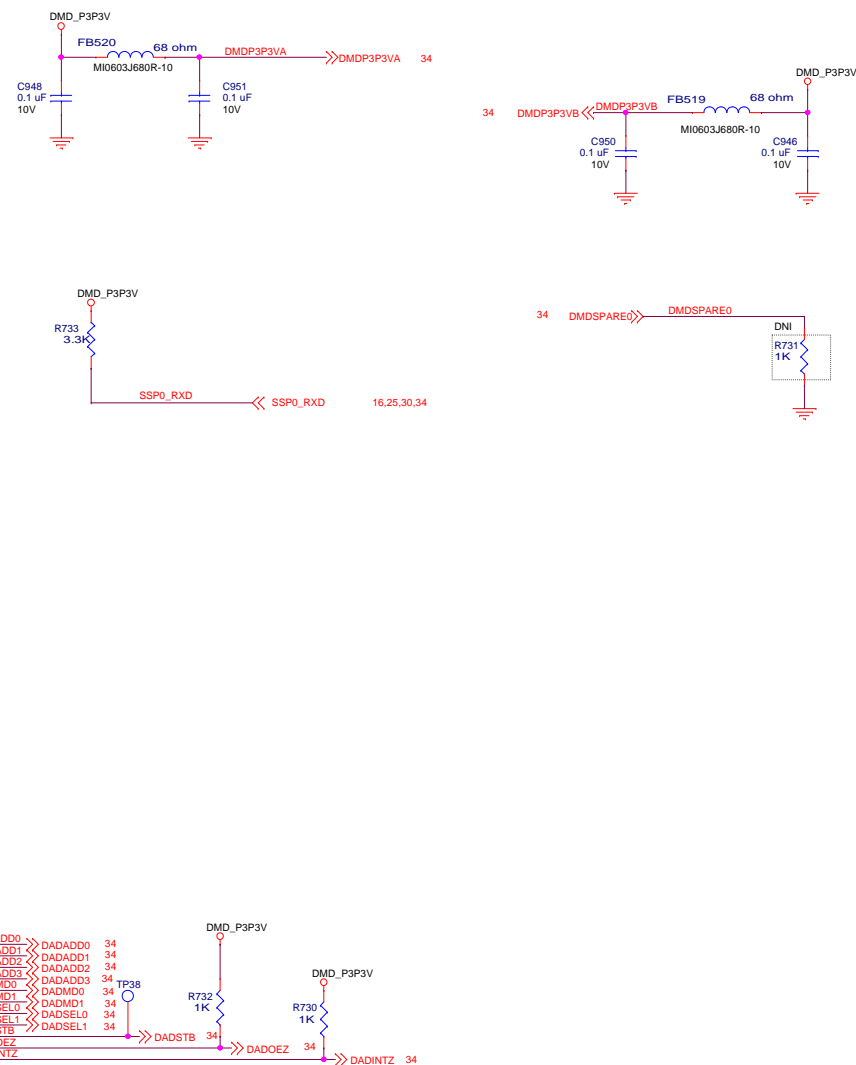
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Primary and Secondary Front End Interface

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				SCALE	SHEET 130F 36

U33B

DOB_P_15	N1	M_DDA00_P	M_DDA00_P	34
DOB_N_15	N2	M_DDA00_N	M_DDA00_N	34
DOB_N_14	N3	M_DDA01_P	M_DDA01_P	34
DOB_N_14	N4	M_DDA01_N	M_DDA01_P	34
DOB_P_14	M2	M_DDA02_P	M_DDA01_N	34
DOB_P_13	M1	M_DDA02_P	M_DDA02_P	34
DOB_N_13	M3	M_DDA03_P	M_DDA02_N	34
DOB_P_12	M4	M_DDA03_N	M_DDA03_P	34
DOB_N_12	L1	M_DDA04_P	M_DDA03_N	34
DOB_P_11	L2	M_DDA04_P	M_DDA04_P	34
DOB_N_11	L3	M_DDA05_P	M_DDA04_N	34
DOB_P_10	L4	M_DDA05_N	M_DDA05_P	34
DOB_N_10	K1	M_DDA06_P	M_DDA06_N	34
DOB_P_9	K2	M_DDA06_N	M_DDA06_P	34
DOB_N_9	K3	M_DDA07_P	M_DDA06_N	34
DOB_P_8	K4	M_DDA07_N	M_DDA07_P	34
DOB_N_8	H1	M_DDA08_P	M_DDA07_N	34
DOB_P_7	H2	M_DDA08_N	M_DDA08_P	34
DOB_N_7	H3	M_DDA09_P	M_DDA08_N	34
DOB_P_6	H4	M_DDA09_P	M_DDA09_P	34
DOB_N_6	G1	M_DDA10_P	M_DDA09_N	34
DOB_P_5	G2	M_DDA10_N	M_DDA10_P	34
DOB_N_5	G3	M_DDA11_P	M_DDA10_N	34
DOB_P_4	G4	M_DDA11_N	M_DDA11_P	34
DOB_N_4	F1	M_DDA12_P	M_DDA11_N	34
DOB_P_3	F2	M_DDA12_N	M_DDA12_P	34
DOB_N_3	F3	M_DDA13_P	M_DDA12_N	34
DOB_P_2	F4	M_DDA13_N	M_DDA13_P	34
DOB_N_2	E1	M_DDA14_P	M_DDA13_N	34
DOB_P_1	E2	M_DDA14_N	M_DDA14_P	34
DOB_N_1	D1	M_DDA15_P	M_DDA14_N	34
DOB_P_0	D2	M_DDA15_N	M_DDA15_P	34
DOB_N_0			M_DDA15_N	34
DDA_P_15	P4	M_DDB00_P	M_DDB00_P	34
DDA_N_15	P3	M_DDB00_N	M_DDB00_N	34
DDA_N_15	P2	M_DDB01_P	M_DDB00_N	34
DDA_P_14	P1	M_DDB01_N	M_DDB01_P	34
DDA_N_14	R4	M_DDB01_P	M_DDB01_N	34
DDA_P_13	R3	M_DDB02_N	M_DDB02_P	34
DDA_N_13	R2	M_DDB03_P	M_DDB02_N	34
DDA_P_12	R1	M_DDB03_N	M_DDB03_P	34
DDA_N_12	T4	M_DDB04_P	M_DDB03_N	34
DDA_P_11	T3	M_DDB04_N	M_DDB04_P	34
DDA_N_11	T2	M_DDB05_P	M_DDB04_N	34
DDA_P_10	T1	M_DDB05_N	M_DDB05_P	34
DDA_N_10	U4	M_DDB06_P	M_DDB05_N	34
DDA_P_9	U3	M_DDB06_N	M_DDB06_P	34
DDA_N_9	U2	M_DDB07_P	M_DDB06_N	34
DDA_P_8	U1	M_DDB07_N	M_DDB07_P	34
DDA_N_8	W4	M_DDB08_P	M_DDB07_N	34
DDA_P_7	W3	M_DDB08_N	M_DDB08_P	34
DDA_N_7	W2	M_DDB09_P	M_DDB08_N	34
DDA_P_6	W1	M_DDB09_N	M_DDB09_P	34
DDA_N_6	Y2	M_DDB10_P	M_DDB09_N	34
DDA_P_5	Y1	M_DDB10_N	M_DDB10_P	34
DDA_N_5	Y4	M_DDB11_P	M_DDB10_N	34
DDA_P_4	Y3	M_DDB11_N	M_DDB11_P	34
DDA_N_4	AA2	M_DDB12_P	M_DDB11_N	34
DDA_P_3	AA4	M_DDB13_P	M_DDB12_P	34
DDA_N_3	AA1	M_DDB13_N	M_DDB12_N	34
DDA_P_2	AA3	M_DDB13_N	M_DDB13_P	34
DDA_N_2	AB2	M_DDB14_P	M_DDB13_N	34
DDA_P_1	AB1	M_DDB15_N	M_DDB14_P	34
DDA_N_1	AC2	M_DDB15_P	M_DDB14_N	34
DDA_P_0	AC1	M_DDB15_N	M_DDB15_P	34
DDA_N_0			M_DDB15_N	34
DCKB_P	J3	M_SCDLKA_P	M_SCDLKA_P	34
DCKB_N	V4	M_SCDLKB_P	M_SCDLKA_N	34
DCKA_P	V3	M_SCDLKB_N	M_SCDLKB_P	34
DCKA_N	J1	M_SCDLRLA_P	M_SCDLKB_N	34
SCB_P	J2	M_SCDLRLA_N	M_SCDLRLA_P	34
SCB_N	V2	M_SCDLRLB_P	M_SCDLRLA_N	34
SCA_P	V1	M_SCDLRLB_N	M_SCDLRLB_P	34
SCA_N			M_SCDLRLB_N	34
DADADDR_0	AB8	DA0	R689	22
DADADDR_1	AF4	DA1	R153	22
DADADDR_2	AE5	DA2	R151	22
DADADDR_3	AD6	DA3	R701	22
DADMODE_0	AE6	DM0	R148	22
DADMODE_1	AD7	DM1	R699	22
DADMODE_2	AC7	DM2	R707	22
DADSEL_0	AE4	DS1	R156	22
DADSEL_1	AF5	OSTB	R150	22
DADSTRB	AE7	DCR2	R68	



Primary Controller DMD Flex Interface

U32B

DDB_P_15	N1	S_DDA00_P	S_DDA00_P	34
DDB_N_15	N2	S_DDA00_N	S_DDA00_N	34
DDB_P_14	N3	S_DDA01_P	S_DDA01_P	34
DDB_N_14	N4	S_DDA01_N	S_DDA01_N	34
DDB_P_13	M1	S_DDA02_N	S_DDA02_P	34
DDB_N_13	M3	S_DDA03_P	S_DDA02_N	34
DDB_P_12	M4	S_DDA03_N	S_DDA03_P	34
DDB_N_12	L1	S_DDA04_P	S_DDA03_N	34
DDB_P_11	L2	S_DDA04_N	S_DDA04_P	34
DDB_N_11	L3	S_DDA05_P	S_DDA04_N	34
DDB_P_10	L4	S_DDA05_N	S_DDA05_P	34
DDB_N_10	K1	S_DDA06_P	S_DDA05_N	34
DDB_P_9	K2	S_DDA06_N	S_DDA06_P	34
DDB_N_9	K3	S_DDA07_P	S_DDA06_N	34
DDB_P_8	K4	S_DDA07_N	S_DDA07_P	34
DDB_N_8	H1	S_DDA08_P	S_DDA07_N	34
DDB_P_7	H2	S_DDA08_N	S_DDA08_P	34
DDB_N_7	H3	S_DDA09_P	S_DDA08_N	34
DDB_P_6	H4	S_DDA09_N	S_DDA09_P	34
DDB_N_6	G1	S_DDA10_P	S_DDA09_N	34
DDB_P_5	G2	S_DDA10_N	S_DDA10_P	34
DDB_N_5	G3	S_DDA11_P	S_DDA10_N	34
DDB_P_4	G4	S_DDA11_N	S_DDA11_P	34
DDB_N_4	F1	S_DDA12_P	S_DDA11_N	34
DDB_P_3	F2	S_DDA12_N	S_DDA12_P	34
DDB_N_3	F3	S_DDA13_P	S_DDA12_N	34
DDB_P_2	F4	S_DDA13_N	S_DDA13_P	34
DDB_N_2	E1	S_DDA14_P	S_DDA13_N	34
DDB_P_1	E2	S_DDA14_N	S_DDA14_P	34
DDB_N_1	D1	S_DDA15_P	S_DDA14_N	34
DDB_P_0	D2	S_DDA15_N	S_DDA15_P	34
DDB_N_0				
DDA_P_15	P3	S_DDB00_N	S_DDB00_P	34
DDA_N_15	P2	S_DDB01_P	S_DDB00_N	34
DDA_P_14	P1	S_DDB01_N	S_DDB01_P	34
DDA_N_14	R4	S_DDB02_P	S_DDB01_N	34
DDA_P_13	R3	S_DDB02_N	S_DDB02_P	34
DDA_N_13	R2	S_DDB03_P	S_DDB02_N	34
DDA_P_12	R1	S_DDB03_N	S_DDB03_P	34
DDA_N_12	T4	S_DDB04_P	S_DDB03_N	34
DDA_P_11	T3	S_DDB04_N	S_DDB04_P	34
DDA_N_11	T2	S_DDB05_P	S_DDB04_N	34
DDA_P_10	T1	S_DDB05_N	S_DDB05_P	34
DDA_N_10	U4	S_DDB06_P	S_DDB05_N	34
DDA_P_9	U3	S_DDB06_N	S_DDB06_P	34
DDA_N_9	U2	S_DDB07_P	S_DDB06_N	34
DDA_P_8	U1	S_DDB07_N	S_DDB07_P	34
DDA_N_8	W4	S_DDB08_P	S_DDB07_N	34
DDA_P_7	W3	S_DDB08_N	S_DDB08_P	34
DDA_N_7	W2	S_DDB09_P	S_DDB08_N	34
DDA_P_6	W1	S_DDB09_N	S_DDB09_P	34
DDA_N_6	Y2	S_DDB10_P	S_DDB09_N	34
DDA_P_5	Y1	S_DDB10_N	S_DDB10_P	34
DDA_N_5	Y4	S_DDB11_P	S_DDB10_N	34
DDA_P_4	Y3	S_DDB11_N	S_DDB11_P	34
DDA_N_4	AA2	S_DDB12_P	S_DDB11_N	34
DDA_P_3	AA1	S_DDB12_N	S_DDB12_P	34
DDA_N_3	AA4	S_DDB13_P	S_DDB12_N	34
DDA_P_2	AA3	S_DDB13_N	S_DDB13_P	34
DDA_N_2	AB2	S_DDB14_P	S_DDB13_N	34
DDA_P_1	AB1	S_DDB14_N	S_DDB14_P	34
DDA_N_1	AC2	S_DDB15_P	S_DDB14_N	34
DDA_P_0	AC1	S_DDB15_N	S_DDB15_P	34
DDA_N_0				
DCKB_P	J3	S_DCLKA_P	S_DCLKA_P	34
DCKB_N	J4	S_DCLKA_N	S_DCLKA_N	34
DCKA_P	V4	S_DCLKB_P	S_DCLKB_P	34
DCKA_N	V3	S_DCLKB_N	S_DCLKB_N	34
SCB_P	J1	S_SCTRLA_P	S_DCLKB_N	34
SCB_N	J2	S_SCTRLA_N	S_SCTRLA_P	34
SCA_P	V1	S_SCTRLB_P	S_SCTRLB_P	34
SCA_N			S_SCTRLB_N	34
DADADDR_0	AF4			
DADADDR_1	AE5			
DADADDR_2	AD6			
DADADDR_3	AE6			
DADM00E_0	AD7			
DADM00E_1	AC7			
DADSEL_0	AE4			
DADSEL_1	AF5			
DADSTRB	AE7			
DAD0EZ	AC8			
DAD_INTZ				

DMD INTERFACE

DLPC4420 Secondary



Secondary Controller DMD Flex Interface

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DWN Oscar Guevara DATE
ISSUE DATE

A3

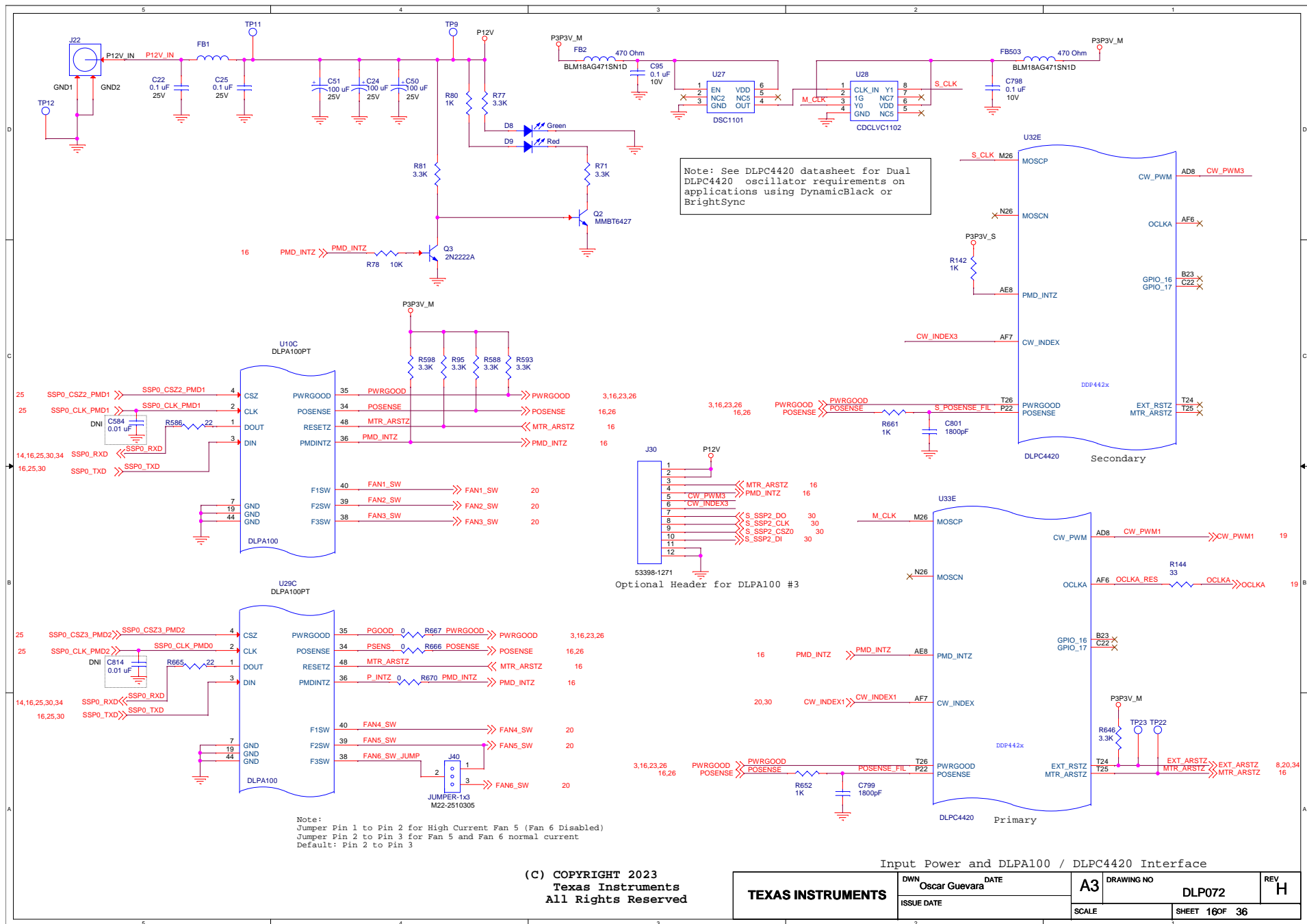
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SCALE

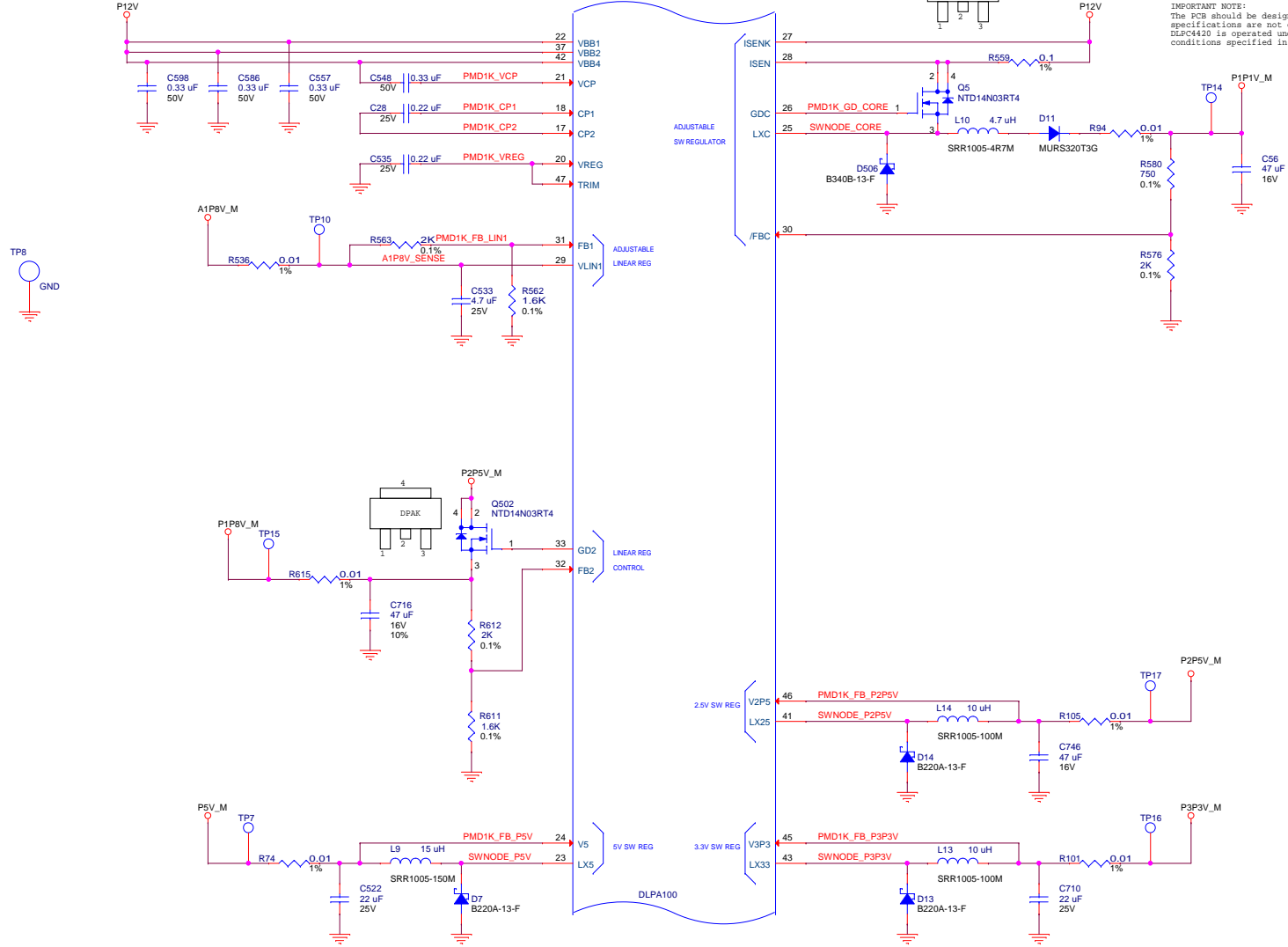
SHEET 150F 36



NOTE:
R620, R634, R69, R102, R131, R85 are used
for current measurement and are not required for
production units.
R713, R100, R232, R638 and R685 are used for alternate
lab supplies and are not required for production units.

NOTE:
Consult the DLP4100 Data Sheet for
external component specifications.

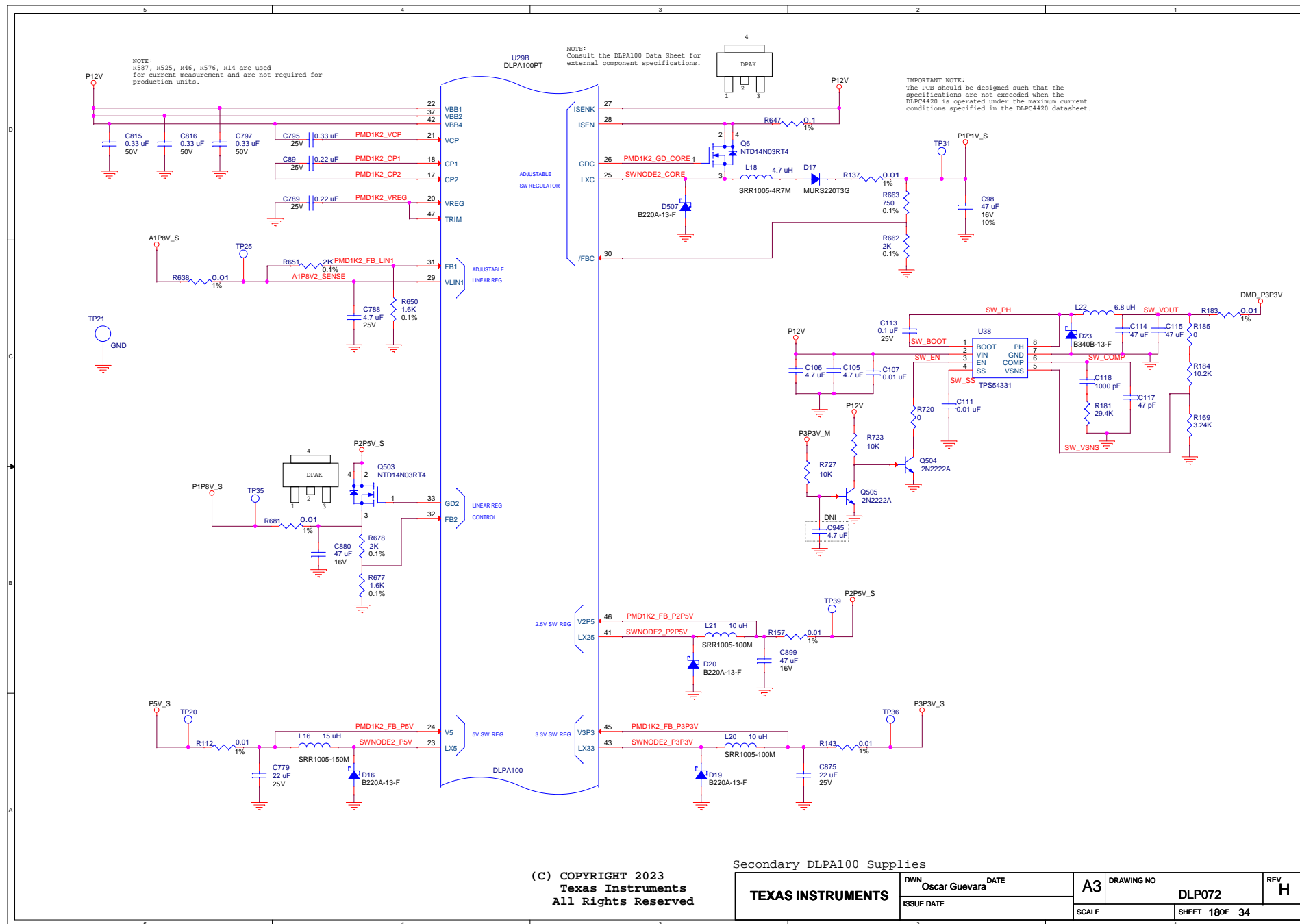
IMPORTANT NOTE:
The PCS should be designed such that the
specifications are not exceeded when the
DLP4100 is operated under the maximum current
conditions specified in the DLP4100 datasheet.



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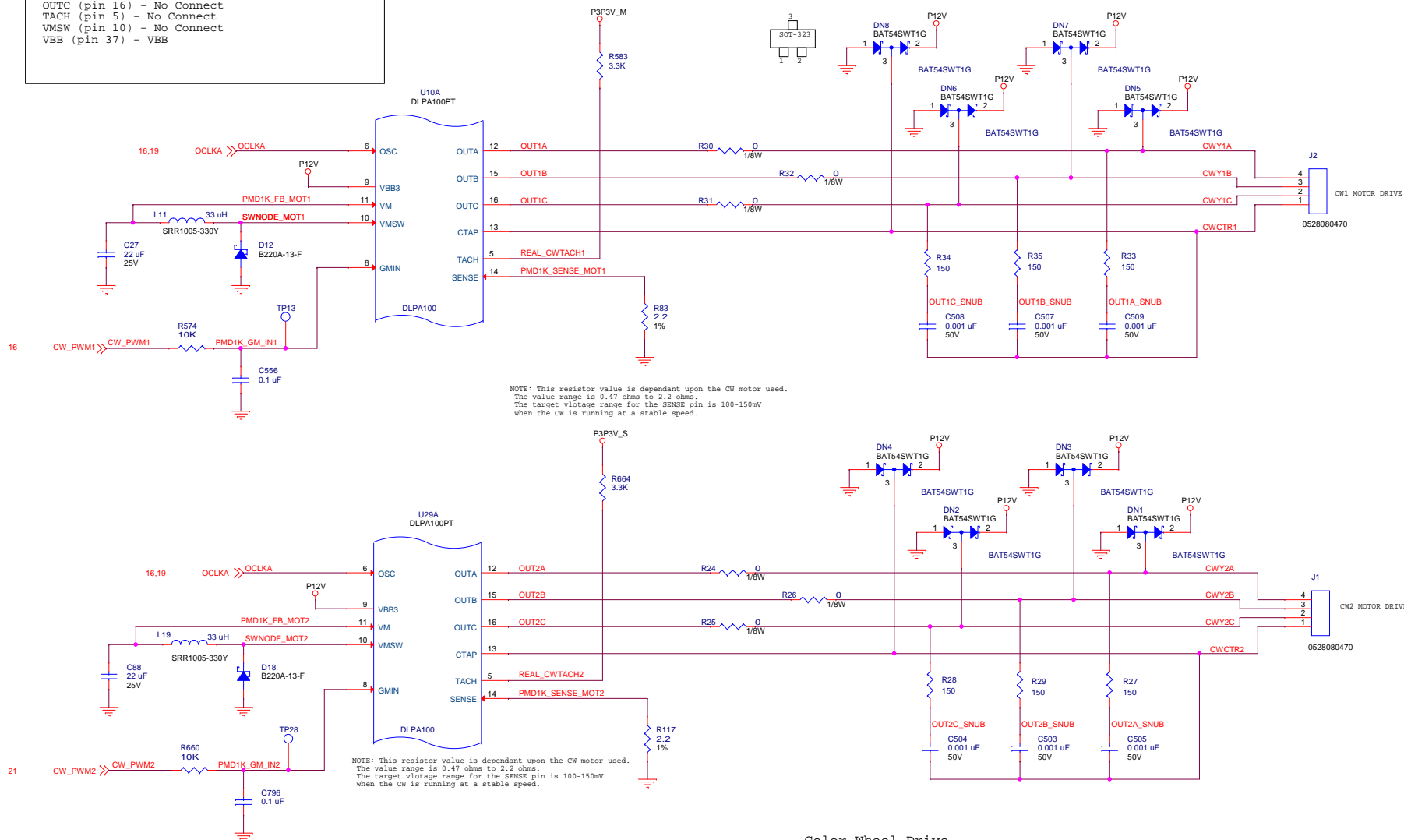
Primary DLP4100 Power Supplies

TEXAS INSTRUMENTS	DWN Oscar Guevara	DATE	A3	DRAWING NO DLP072		REV H
	ISSUE DATE					
				SCALE	SHEET 17 OF 36	



Note: If not using the motor driver on the DPLA100 follow these guidelines for unused pins:

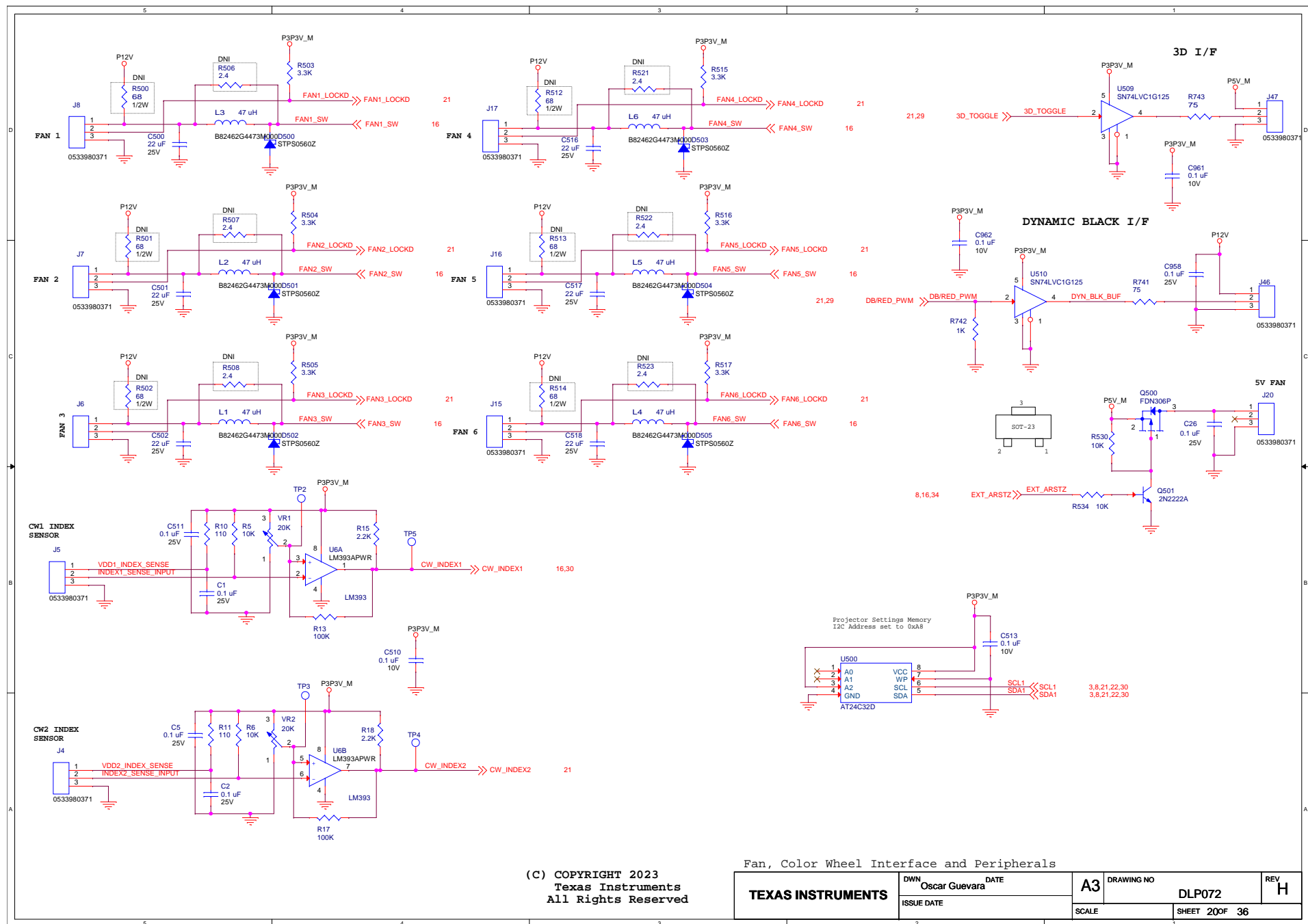
- GMIN (pin 8) - Ground
- OSC (pin 6) - Ground
- SENSE (pin 14) - Ground
- CTAP (pin 13) - VBB
- VM (pin 11) - VBB
- OUTA (pin 12) - No Connect
- OUTB (pin 15) - No Connect
- OUTC (pin 16) - No Connect
- TACH (pin 5) - No Connect
- VMSW (pin 10) - No Connect
- VBB (pin 37) - VBB

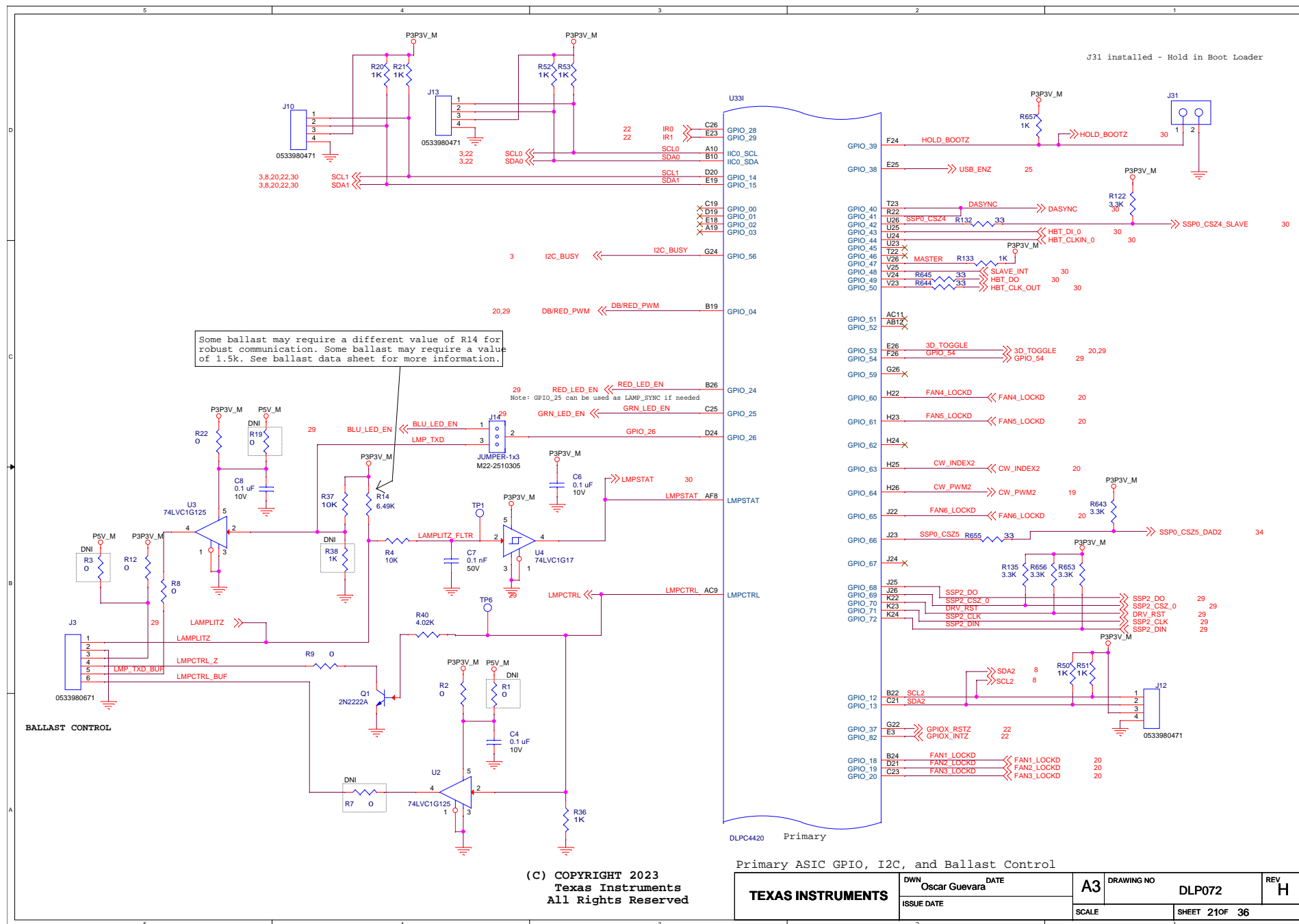


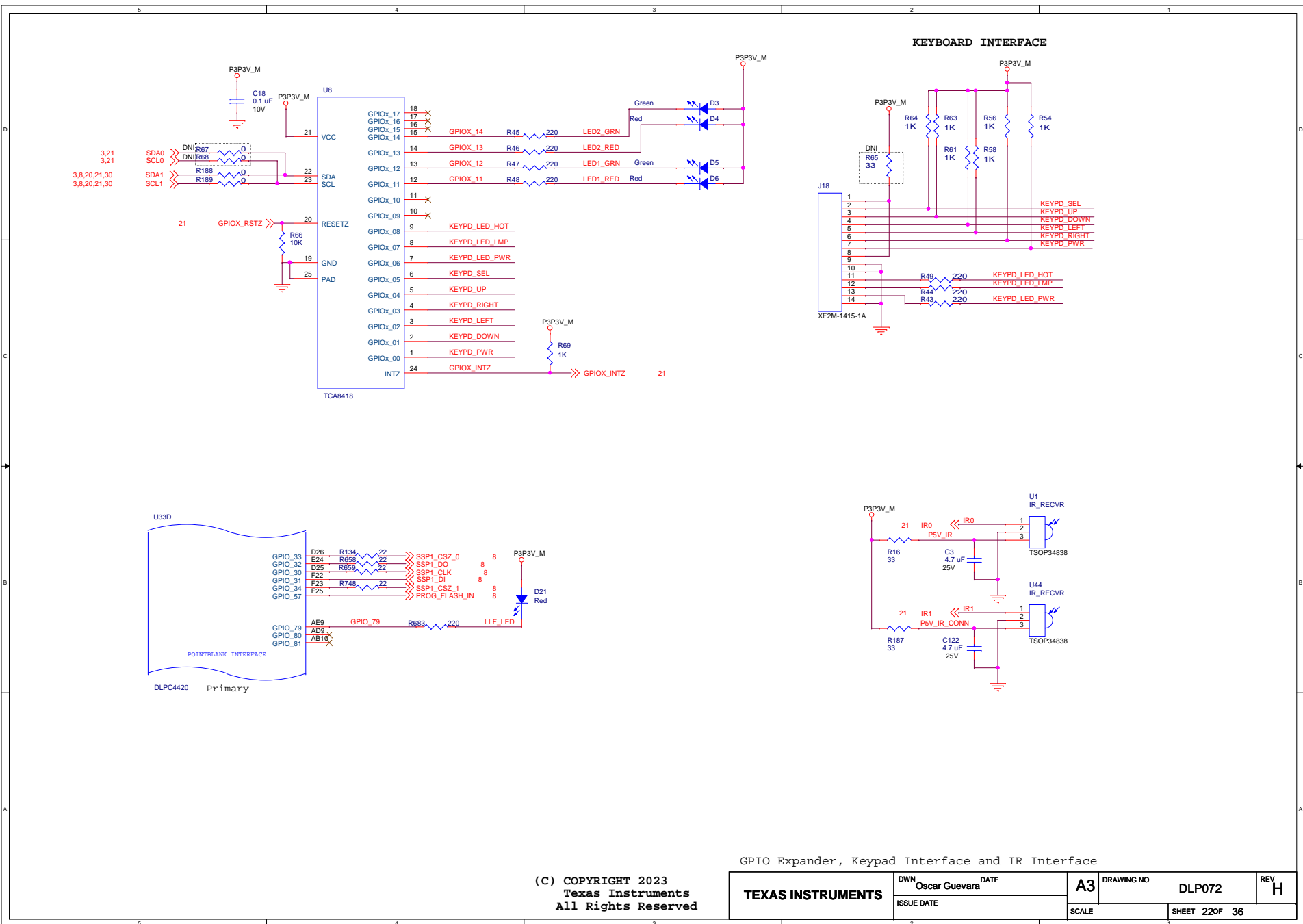
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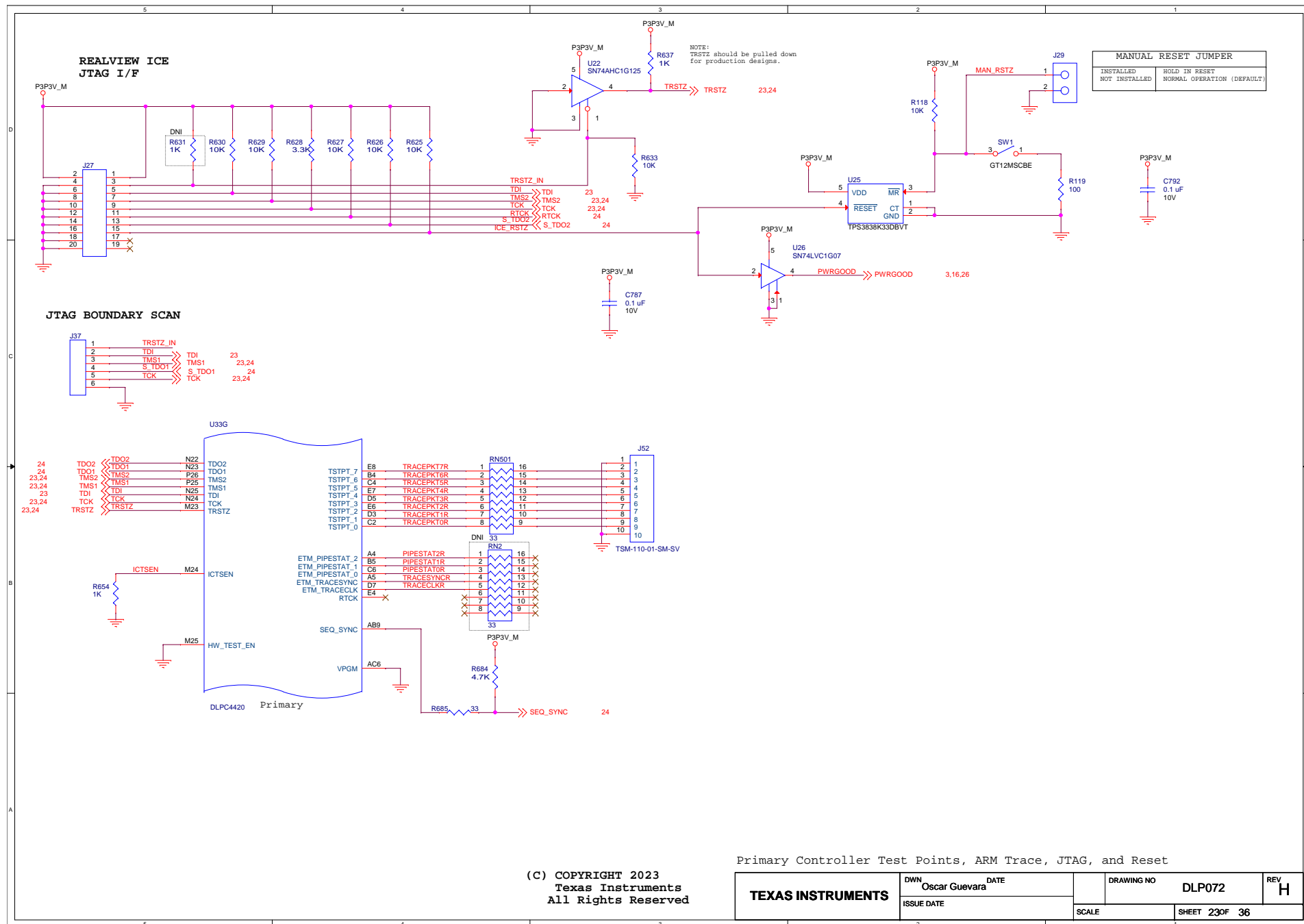
Color Wheel Drive

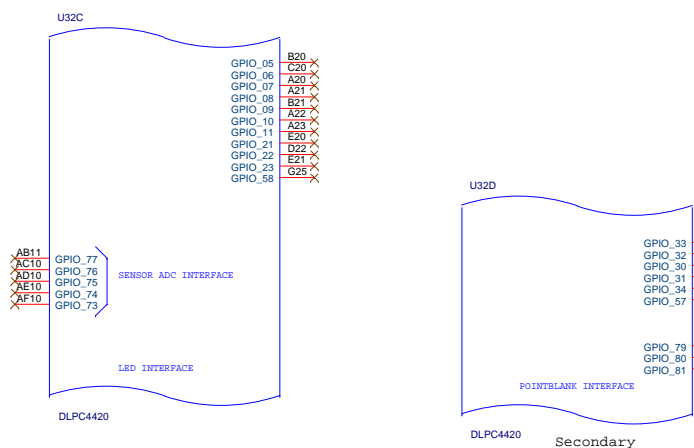
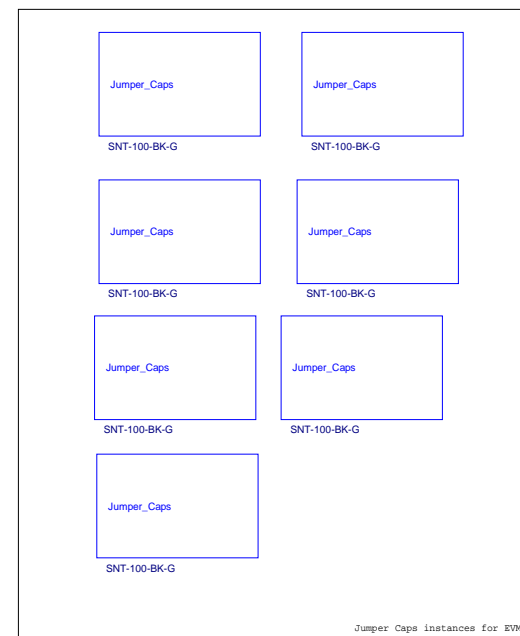
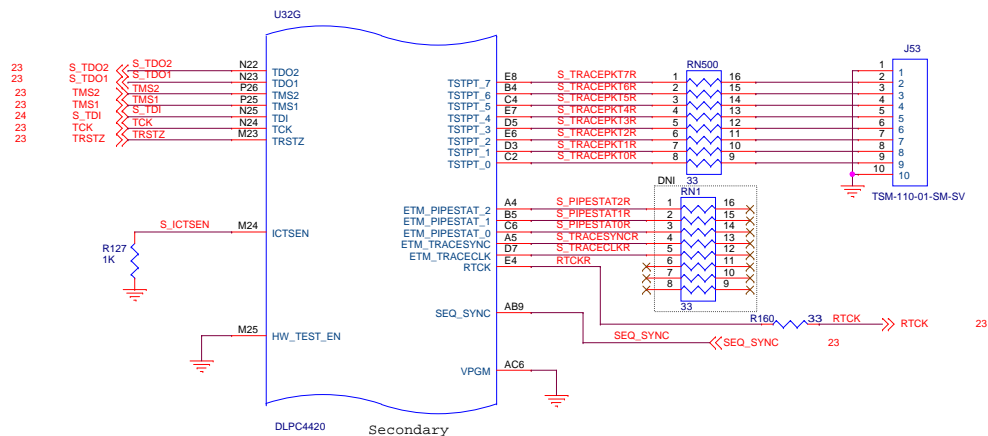
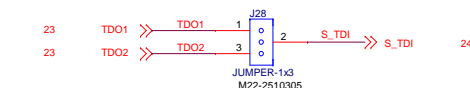
TEXAS INSTRUMENTS	DWN Oscar Guevara	DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE	SCALE			











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Secondary Controller Test Points, ARM Trace, and JTAG

TEXAS INSTRUMENTS

DWN Oscar Guevara DATE
ISSUE DATE

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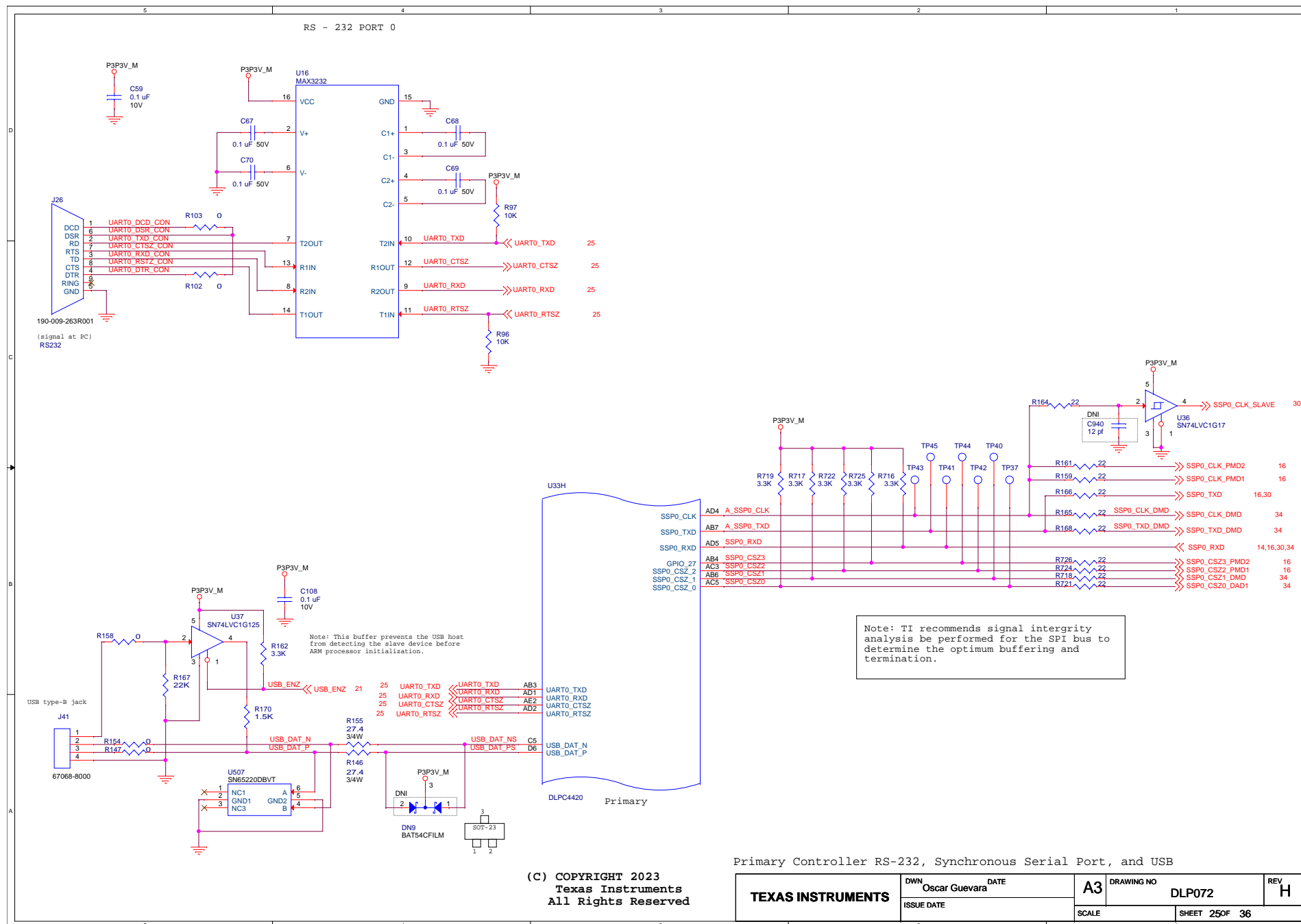
DLP072

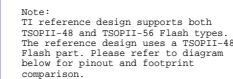
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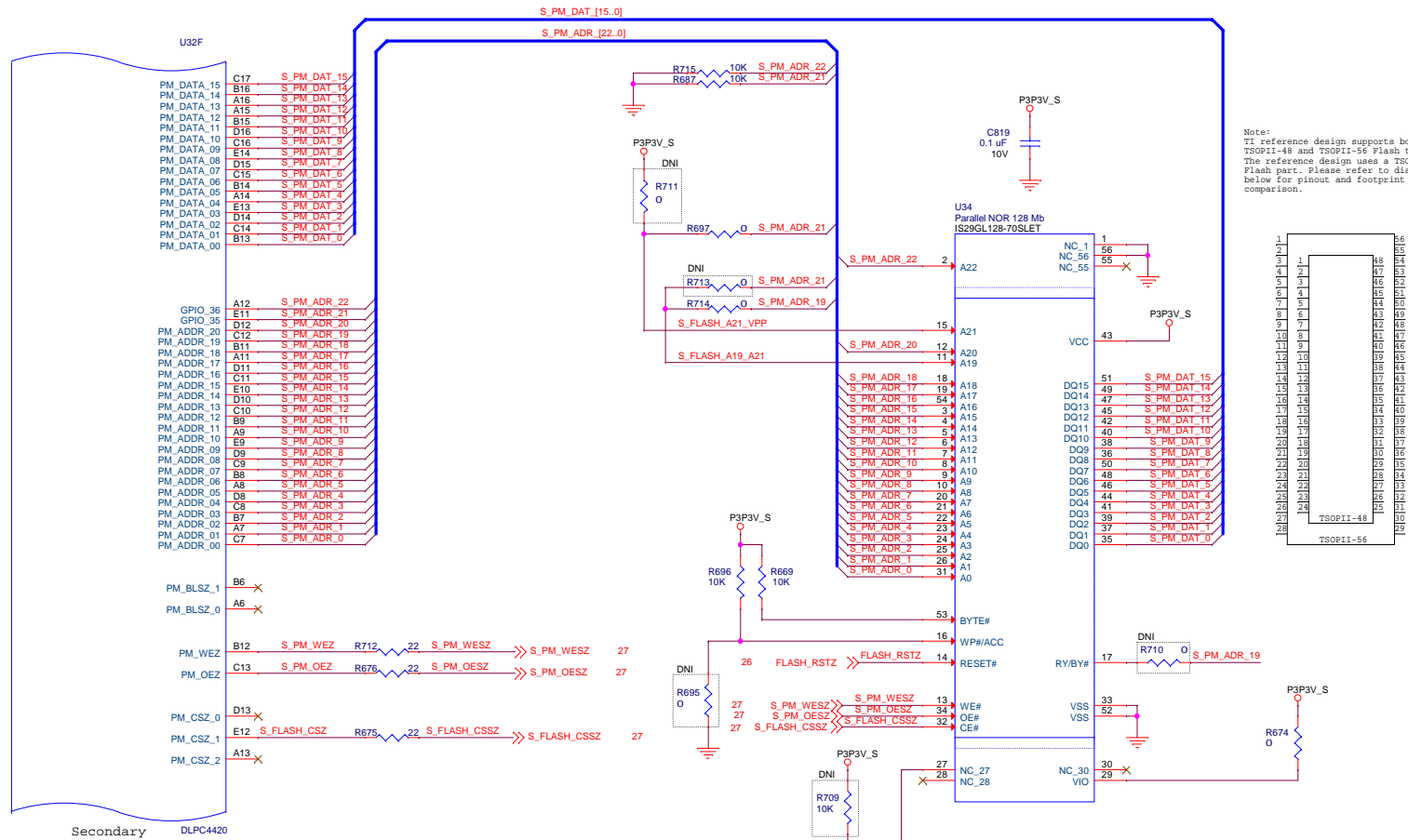
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SHEET 240F 34





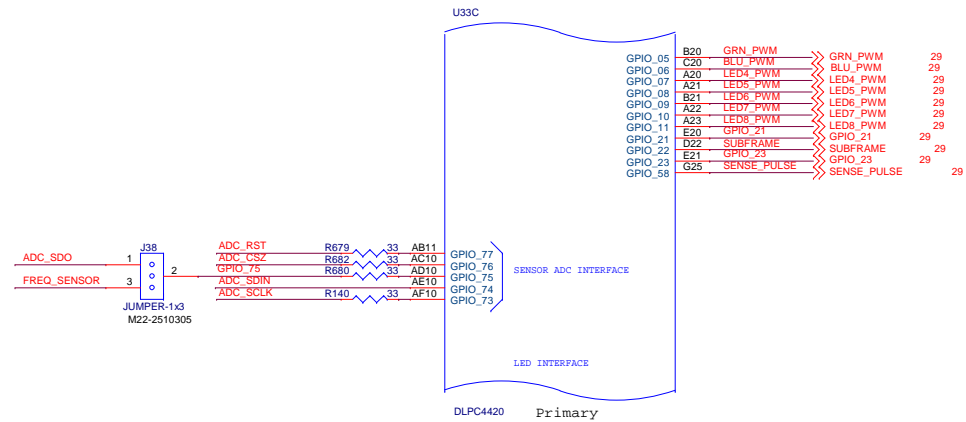
SCALE	SHEET 26 OF 36
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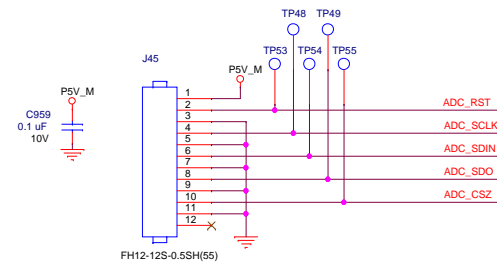
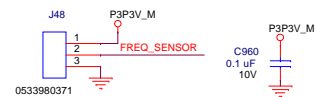
Secondary Controller Flash Memory Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara	DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE				
			SCALE	SHEET 27OF 36	



ADC INTEGRATING SENSOR BOARD I/F

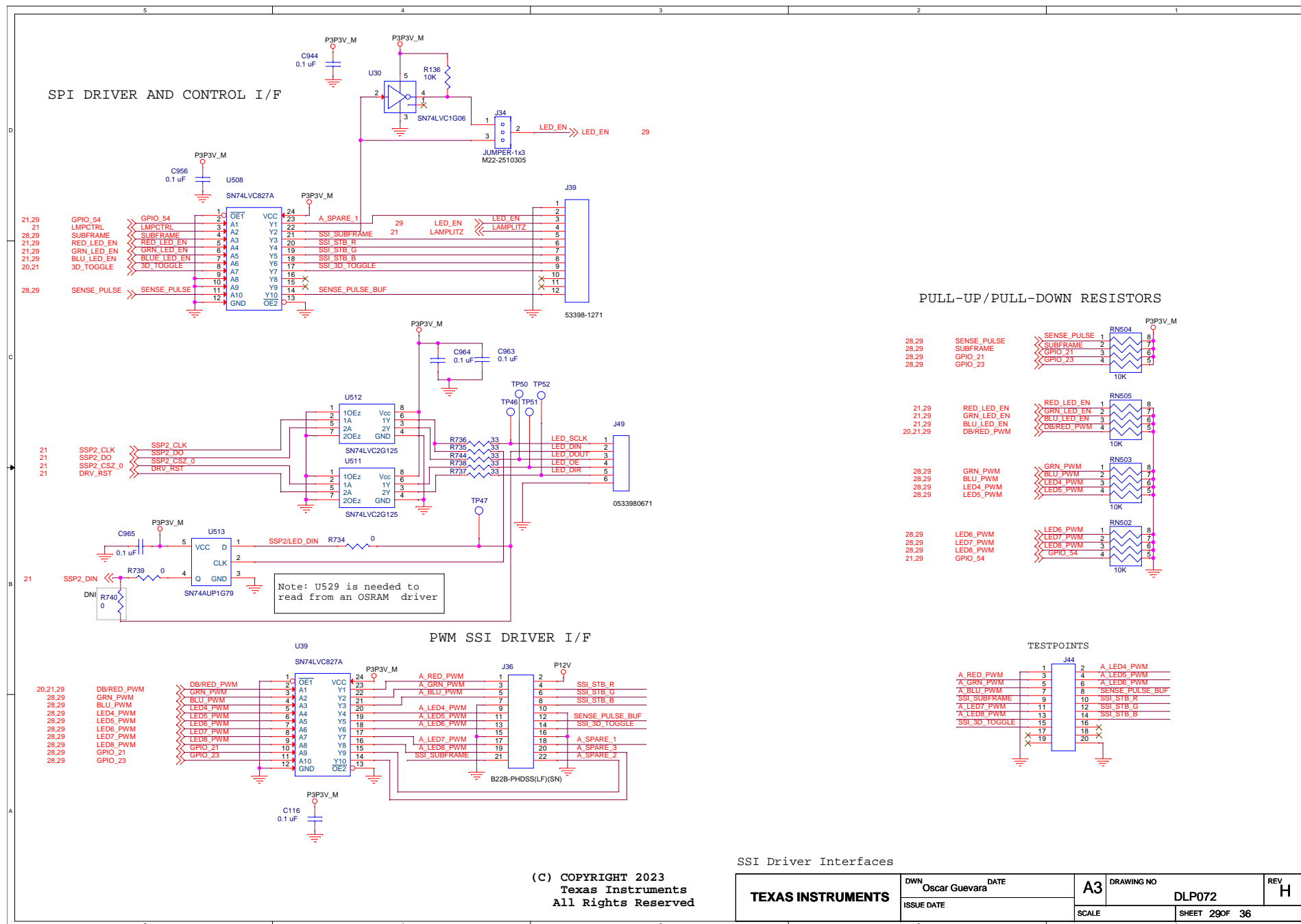
LIGHT TO FREQUENCY SENSOR I/F

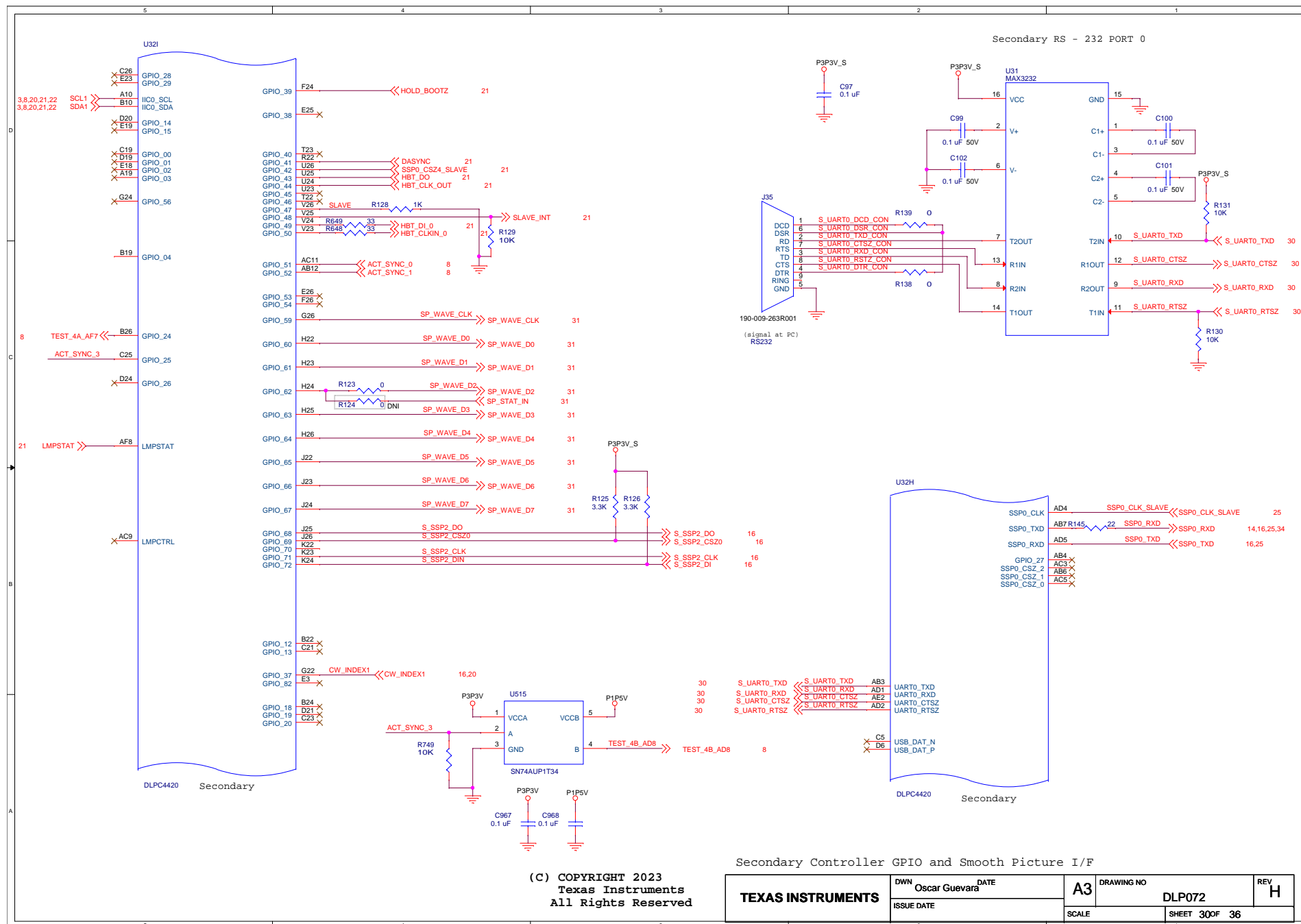


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Primary Controller SSI Sensor Interface

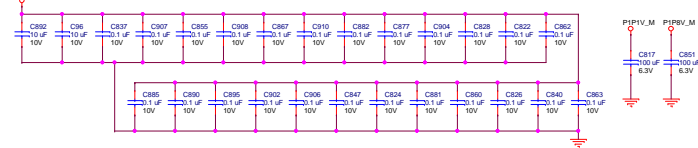
TEXAS INSTRUMENTS	DWN Oscar Guevara	DATE	A3	DRAWING NO	DLP072	REV	H
	ISSUE DATE		SCALE	SHEET	280F	36	



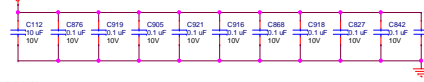


SCALE	SHEET 31 OF 36
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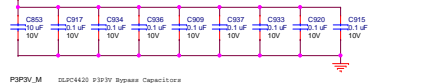
P1P1V_M DLP4420 P1P1V Bypass Capacitors



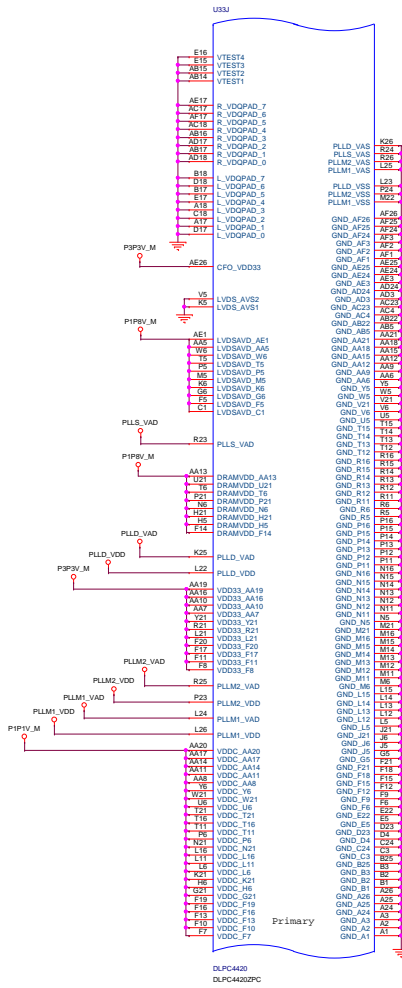
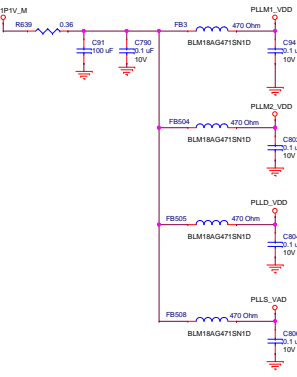
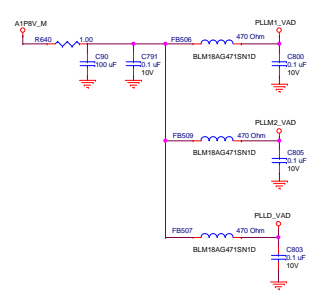
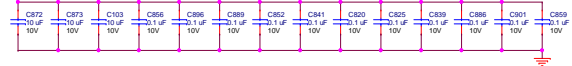
P1P1V_M DLP4420 P1P1V LVDS Bypass Capacitors



P1P1V_M DLP4420 P1P1V OSAR Bypass Capacitors



P1P1V_M DLP4420 P1P1V Bypass Capacitors



Primary Controller Power and Bypass Capacitors

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		ISSUE DATE	02/09/2023		DLP072	H
		SCALE			SHEET 32 OF 36	

Revision A:
Initial Release

Revision B:
All Pages: Resequenced reference designators to align with layout
Page 1: Updated notes with correct voltage names
Updated index
Page 4: Rearranged DDR3_1_DQ[15:0] for routability

Revision C:
Page 3: Change U5 to Do Not Install
Updated C545 and C549 as Do Not Install
Changed U506 to 75 Mhz
Page 11: Added Note Connecting pin 15 of U24 to P3P3V
Page 8: Changed R89, R90, R91, R92, and R541 to 0 ohms.

Revision D:
Page 3: Changed net name TEST_4A_AC6 to VX1_3D_EN.
Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page 8: Added R190, R191, R192, and R193.
Changed net name TEST_4A_AC6 to VX1_3D_EN.
Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page 11: Connected pin 15 of U24 to P3P3V.
Page 16: Changed C799 and C801 to 1800pF.
Page 21: Added note to ballast circuit.
Page 22: Added R188 and R189.
Page 23: Changed RN501 to Install, added J52 header.
Page 24: Changed RN500 to Install, added J53 header.

Revision E:
Page 11: Changed U24-10, C85 connection from P3P3V to P5V_S.

Revision F:
Page 3: Added U514, Y1, R745, R746, R747, C966
Page 3: Removed FB502, C534, U506
Page 8: Added J54, J55, and J56
Page 22: Added R748 and connection to GPIO_34

Revision G:
Page 8: Added Off-Page connections to TEST_4A_AF7 and TEST_4B_AD8.
Page 30: Added TEST_4A_AF7 connection to GPIO_24 on U32

Revision H:
Page 3: Updated FE_12V to RE_5V
Removed nets: "USB+5V", "USB_D+", "USB_D-"
Added I2C nets "SCL1", "SDA1"
Rearraged nets "VX1_LR_SYNC", "FE_RST", "SDA0", "I2C_BUSY"
Page 14: Removed J51
Page 15: Removed J50
Page 34: Added J57 FMC Connector

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TEXAS INSTRUMENTS

DWN	Oscar Guevara	DATE
ISSUE DATE		

A3	DRAWING NO
DLP072	

REV
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SCALE	SHEET 35 OF 36
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TEXAS INSTRUMENTS	DWN Oscar Guevara	DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE				
				SCALE	SHEET 36 OF 36